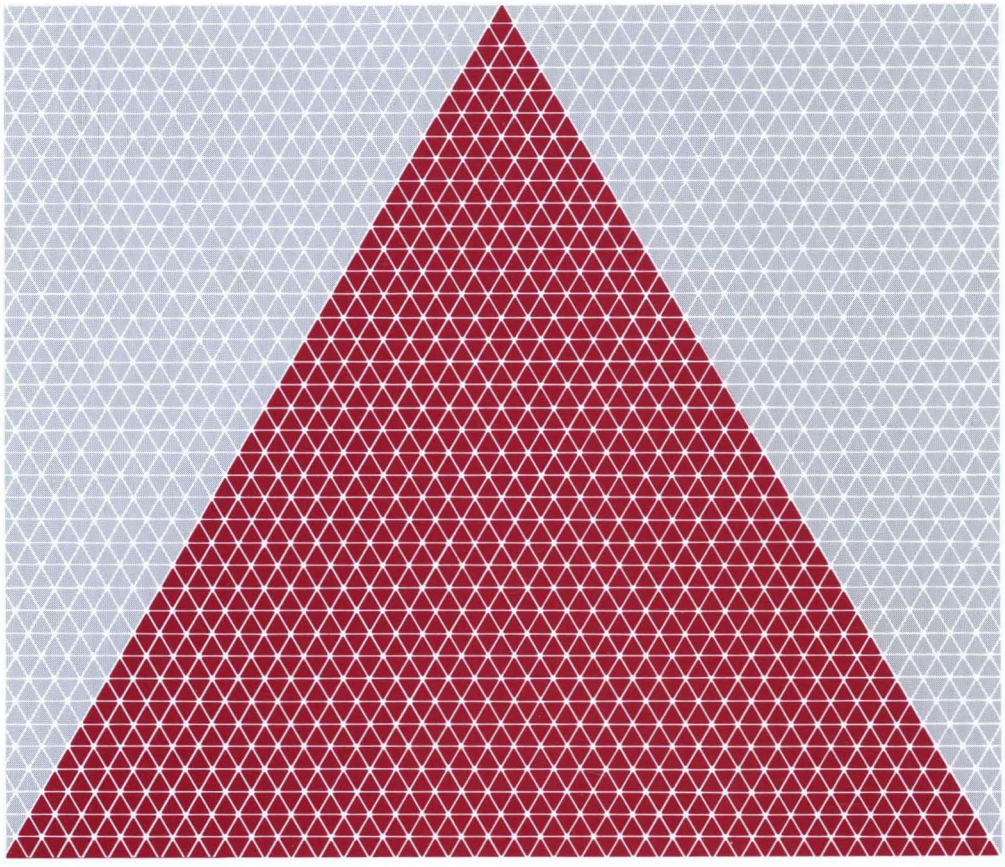
Altos Computer Systems

386 Series 2000
Field Service



Altos Computer Systems

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386 Series 2000
Field Service

Document History

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This equipment is intended for commercial use only and is not suited for operation in Class B environments.

The use of shielded I/O cables is required when connecting the equipment to any and all optional peripheral or host devices. Failure to do so may violate FCC rules.

About This Manual

This manual contains detailed information for field-service personnel who are trained in digital electronics, microcomputers, and operating systems.

The purpose of this manual is to describe the operation of the Altos 386 Series 2000 Computer System and provide specific information to enable the field-service technician to effectively service the computer system at the customer site.

Careful attention to the maintenance information contained in this manual will ensure maximum trouble-free operation from the system.

This manual is organized into the following parts and chapters:

Part I Overview

Chapter 1 System Description

- describes the features and capabilities of the system
- provides a hardware overview of the major circuits and peripherals
- lists and shows the location of the field replaceable assemblies comprising the system
- describes and shows the dedicated and recommended expansion plug-in printed circuit board locations
- describes and shows the locations of the front and rear-panel controls, connectors, and indicators
- discusses the software available for the system

Chapter 2 Subsystem Operation

- explains how the major subsystems interface to the system through the system bus
- describes how each major subsystem operates

Part II Maintenance

Chapter 3 Power-Up Checks

- provides a guide for determining which diagnostic test procedures to use
- discusses troubleshooting techniques
- includes preliminary trouble analysis information for a dead system
- includes a discussion of the monitor program
- describes the power-up sequence
- provides a description of the power-up tests
- includes trouble-analysis information

Chapter 4 Floppy-Based Diagnostics

- provides instructions for booting the diagnostic floppy disks
- describes the system-confidence (SDX) tests
- describes the field-service (FDX) tests
- includes trouble-analysis information

Chapter 5 Monitor Debugger

- describes the monitor communication protocol and system calls

- describes the debugger tests

Chapter 6 Removal/Replacement

- provides procedures for removing and replacing the field-replaceable units (FRUs)
- includes instructions for shipping FRUs

Chapter 7 Preventive Maintenance

- provides cleaning procedures

Appendices

A Jumpers and Switches. Describes the jumper and switch settings for the system.

B Utilities. Includes procedures for using the utility programs available on the System Diagnostics Executive (SDX) and Field Diagnostics Executive (FDX) floppy disk.

C Loopback Connectors. Illustrates the proper jumper connections for assembling the loopback connectors required to perform the diagnostic procedures.

D System Specifications. Lists the system electtrical, environmental, and physical specifications.

E Storage Device Specifications. Lists detailed manufacturer's specifications for each qualified tape, floppy, and hard disk drive currently used in the system.

F 115/230 VAC Conversion. Provides procedures for converting the system to 115 or 230 volt AC operation.

G Multidrop Cables and Terminators. Provides information for making your own multidrop cables and terminators.

H Power Consumption Chart. Provides power consumption information for the available Series 2000 configurations.

Glossary

Includes an alphabetical list and definitions of specialized terms and acronyms used in this manual.

RELATED PUBLICATIONS

The following is a list of publications that contain information relating to the Series 2000 system. The Altos 386 Series 2000 Owner's Guide is shipped with the Series 2000. The remaining publications are optional and are divided into three types:

- basic (run-time) system manuals for installing and using the operating system
- development system manuals that include reference and tutorial material for programs available in the development system
- supplemental information manuals that are referenced in the text of this manual and contain additional information required to understand the operation of the system. (Includes maintenance manuals required to service the system.)

The publications listed here are available through an Altos distributor or directly from integrated circuit manufacturers.

Shipped With Series 2000

Altos 386 Series 2000 Owner's Guide (Altos part no. 690-20351-xxx)

Basic System

- Installing XENIX (Altos part no. 690-16630-xxx)
- XENIX/UNIX Using the AOM Menu System (Altos part no. 690-18055-xxx)
- XENIX Commands Directory (Altos part no. 690-16640-xxx)

Development System

XENIX Development System Set (Altos part no. 690-18607-xxx)

Supplemental Information

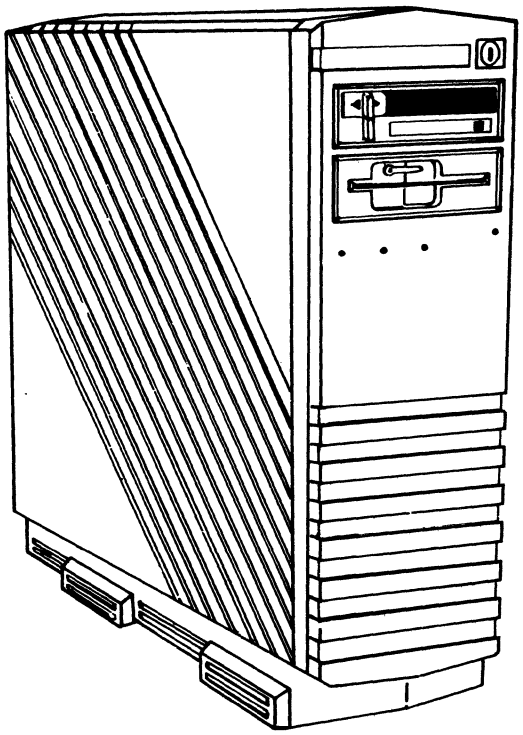
- Altos 386 Series 2000 Maintenance Manual (Altos part no. 690-20652-xxx)
- Altos 386 Series 2000 Illustrated Parts List (Altos part no. 690-xxxxx-xxx)
- Intel IAPX 386 Programmer's Reference Manual
- Intel IAPX 286 Programmer's Reference Manual
- Intel Microsystem Components Handbook
- Motorola 141868A Data Sheet
- Advanced Micro Devices 9517 Technical Data Sheet
- Zilog Data Handbook/Technical Manual
- Zilog Z8536 and Z8530 Technical Reference Manuals
- Siemans SAB82258 ADMA User's Manual
- Hitachi Microcomputer Data Book
- Hitachi HD68450 DMAC Application Notes Handbook
- National Cash Register 5385 SCSI Protocol Controller Data Sheet
- Archive QIC-02 1/4 Inch Tape Drive Interface
- Archive QIC-24 1/4 Inch Cartridge Tape Drive Format
- Archive QIC-36 Basic 1/4 Inch Cartridge Streaming Tape Drive Interface
- NEC Data Handbook

- ANSI X3T9.2/82-2 SCSI Small Computer System Interface
- National Cash Register Data Handbook

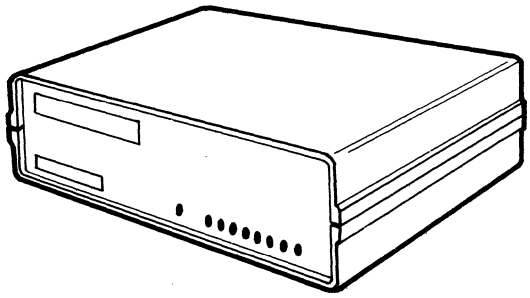
SPECIAL SYMBOLS AND NOTATIONS

The following is a list of the special symbols and notations used in this manual:

Symbol/ Notation	Description
* (Asterisk)	Used following a capitalized mnemonic or signal name to indicate a "not" (complement) function or an active low signal. Example: PERR*
h	Used after a number to indicate that the number is a hexadecimal notation. Example: 25h
d	Used after a number to indicate that the number is a decimal notation. Example: 16d
b	Used after a number to indicate that the number is a binary notation. Example: 01b



COMPUTER



TERMINAL CLUSTER UNIT

01310

Altos 386 Series 2000 Computer System

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System Description

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INTRODUCTION

This chapter describes the Altos 386 Series 2000 Computer System. The Series 2000 is a compact floor-standing computer system designed for general processing, office automation, and network fileserver applications. The Series 2000 computer contains the following major subsystems:

- CPU board
- memory board
- multidrop and/or SIO communications boards
- file processor board
- ESDI controller board
- streaming tape drive
- floppy disk drive
- ESDI hard disk drive(s)

Features

- modular architecture for easy system expansion
- major functions located on multiple plug-in printed circuit boards for easy service
- high-speed 32-bit expanded Multibus I®
- high-performance 16 MHz Intel 80386 microprocessor
- high-speed Intel 80387 floating-point numeric processor
- up to three 170M byte enhanced small device interface (ESDI) hard disk drives
- multidrop communications that supports multidropped terminals or terminal cluster units (TCUs)

- up to 16M bytes of system memory
- internal 60M byte streaming cartridge tape backup
- storage expansion beyond 510M bytes (unformatted) via a small computer system interface (SCSI) channel
- remote diagnostics available (with optional modem) for rapid fault isolation to field-replaceable units

Architecture

The modular system architecture allows convenient service and system expansion with a wide variety of configurations. The system can contain up to eight plug-in printed-circuit board subsystems and five storage device modules. Five boards are used for the standard system which leaves three spare board slots to use for system expansion.

All of the plug-in boards slide into the back of the chassis and connect to the backplane located in the center of the chassis. The cartridge tape, floppy disk, and up to three hard disk drives are easily installed or replaced by removing the front panel and sliding the drives in or out of the chassis. The hard disk drives plug directly into the backplane.

The backplane serves as the medium for data interchange between the processors, system (RAM) memory, and storage devices.

Configurations

The following three versions of the Series 2000 were available at the date of this publication:

Subsystems	Version 1	2	3
386 CPU	X	X	X
System Memory			
4 MB	X	X	
8 MB			X
SCSI File Processor	X	X	X
ESDI Controller	X	X	X
Communications			
SIO	X		
MDC		X	X
ESDI Hard Disk			
80 MB	X		
170 MB		X	X
Floppy Disk			
1 MB/1.6 MB	X	X	X
Streaming Tape			
60 MB	X	X	X
TCU-8		X	X
Altos V Terminal	X	X	X

A system can be configured with more than one SIO communications board for special applications to allow the system to run a variety of communications protocols, such as, 3270, 3780, X.25, and SNA at the same time (see "Communications" for additional information).

The number of RS-232 I/O ports and the size of the system memory and hard disk storage can be tailored for any particular application. For example, if many external I/O devices (terminals, printers, etc.) are required, but only a few are being used at one

time, the I/O devices may be supported without adding disk storage or system memory.

The Intel 80387 floating-point numeric processor and large amounts of system memory can be used for environments where CPU intensive applications are run with large programs (it takes only two 8M byte memory boards to configure the system with 16M bytes of RAM memory).

Multiple fast-access ESDI hard disk drives can be used for applications that require a large number of disk transactions per second. By using multiple drives, the number of disk transactions per second goes up significantly because of the gains made using overlapped seeks. Thus, a system can be configured with a maximum unformatted storage capacity of 510M bytes.

Networking

The system hardware supports optional local area networking (LAN). The networking hardware runs at 750K and 1.4M bits per second which allows the system to talk to a variety of Altos computer systems. A simple low-cost, twisted-pair, RS-422 interface provides the network media interface.

The Series 2000 can run WorkNet® software that is compatible with other Altos computer systems. The WorkNet software allows transparent remote file access and remote processor execution, which means that any user on the network can share and access files on other systems (as if the files were all on the local disk).

These features make it possible to build large computer installations that support hundreds of users. For example, a network of 10 systems can support 300 users and contain over 51G (giga) bytes of unformatted hard disk storage.

Communications

The multidrop communications board supports multidropped terminals and/or asynchronous RS-232 devices interfaced through terminal cluster units (TCUs) via a 1M bit per second RS-422 interface.

However, operating system licensing allows either 32 (standard) or 64 (optional) bidirectional devices (e.g., terminals) to be logged in at any one time. If more than 32 (or 64) terminals attempt to log in, a message will appear on the disallowed terminal to inform the user that the maximum number of terminals are already logged in.

Currently, up to 64 addressable devices (subject to operating system and license limitations), including the devices directly connected to the asynchronous ports, can be configured on any multidrop communications board. For example, if seven TCU-8s are configured on a single multidrop board, then all the possible addresses will be in use (the four asynchronous ports and the WorkNet port will always require five addresses which leaves 56 addresses for the RS-422 devices on the multidrop trunk line). The multidropped TCU-8 takes up eight of the available addresses even if less than eight RS-232 devices are connected to the TCU-8.

The multidrop communications board requires only one system board slot (instead of the three slots required for three 10-port SIO communications boards) which leaves up to two additional board slots for expansion.

The Series 2000 supports several communications protocols which are down-loaded to the SIO communications board(s). These communications protocols are run by the microprocessor on the communications board(s) which off-load this burden from the main CPU.

NOTE

The multidrop communications board hardware is capable, with the SIO communications board, of running several communications protocols at the same time. However, this capability depends on the availability of the software. The software for running the communications protocols is down-loaded into the local RAM on the SIO communications board.

Altos currently offers bisynchronous communications (BSC) 3270 and 3780, X.25, and 3270 SNA software to run on the Series 2000 with the SIO communications board installed.

The system is capable of supporting asynchronous modems for dial-up data base services or off-site communications and synchronous modems for other emulations. Altos WorkNet I or II is supported through one port at a rate of 1.4M bits per second or 750K bits per second. The SIO communications board subsystem, configured with 128K bytes of RAM, supports certified X.25 or IBM/SNA software protocols.

Terminal Cluster Units

The terminal cluster unit (TCU) connects to the multidrop communications board via a high-speed RS-422 interconnect scheme. The TCU provides a serial interface to any asynchronous RS-232 device at baud rates from 50 to 19,200.

Diagnostics

The Series 2000 performs three major categories of diagnostic tests. The first category is the built-in hardware tests contained in the power-up monitor program. (Refer to "System Software" later in this chapter for additional diagnostics information.)

The second category of tests is the user system-confidence (SDX) tests. The third category is the field-service diagnostics (FDX) tests which can be run from a floppy disk which is available as part of a maintenance package from Altos Customer Support.

Power-Up Tests

The power-up tests are contained in the ROM-based firmware on the CPU, multidrop and/or SIO communications, and file processor boards. These power-up tests are always performed when power is applied to the system to check the minimum hardware configuration on its particular board, identify any missing or failed subassemblies, and then confirm communication with the system.

The CPU power-up tests include cache memory, tag RAM memory, counter/timer I/O (CIO), clock, floating-point numeric processor, interrupt, and system bus checks.

The file processor power-up tests include local RAM and PROM, interval timer, system bus, DMA controller, and storage device controller checks. The multidrop and SIO communications board power-up tests consist of local RAM and PROM, I/O integrated circuits, DMA controller, interrupts, and system bus checks.

System-Confidence Tests

The system-confidence (SDX) tests are menu driven and allow a non-technical user to test the operation of the system.

A full set of tests can be easily run from the system console. System utilities for handling system configuration and storage devices are also included.

Field-Service Diagnostics

More detailed and flexible tests are available for the more experienced user with the field-service (FDX) tests.

The field-service (FDX) tests are supplied on a floppy disk available as part of a maintenance package from Altos Customer Support.

In most multiboard systems, the CPU, system memory, controller, and communications boards must be working before field-service diagnostic testing can start. However, the multidrop or SIO communications board contains a full 16-bit microprocessor that acts as a diagnostic controller on the system bus. Thus, each board can be called up and tested separately, or the full system can be enabled and exercised to isolate and identify failures for repair or replacement.

CONTROLS, CONNECTORS, AND INDICATORS

The following is a description of the Series 2000 computer and terminal cluster unit controls, connectors, and indicators indexed (by number) to the exploded-view illustrations in Figures 1-1 and 1-2.

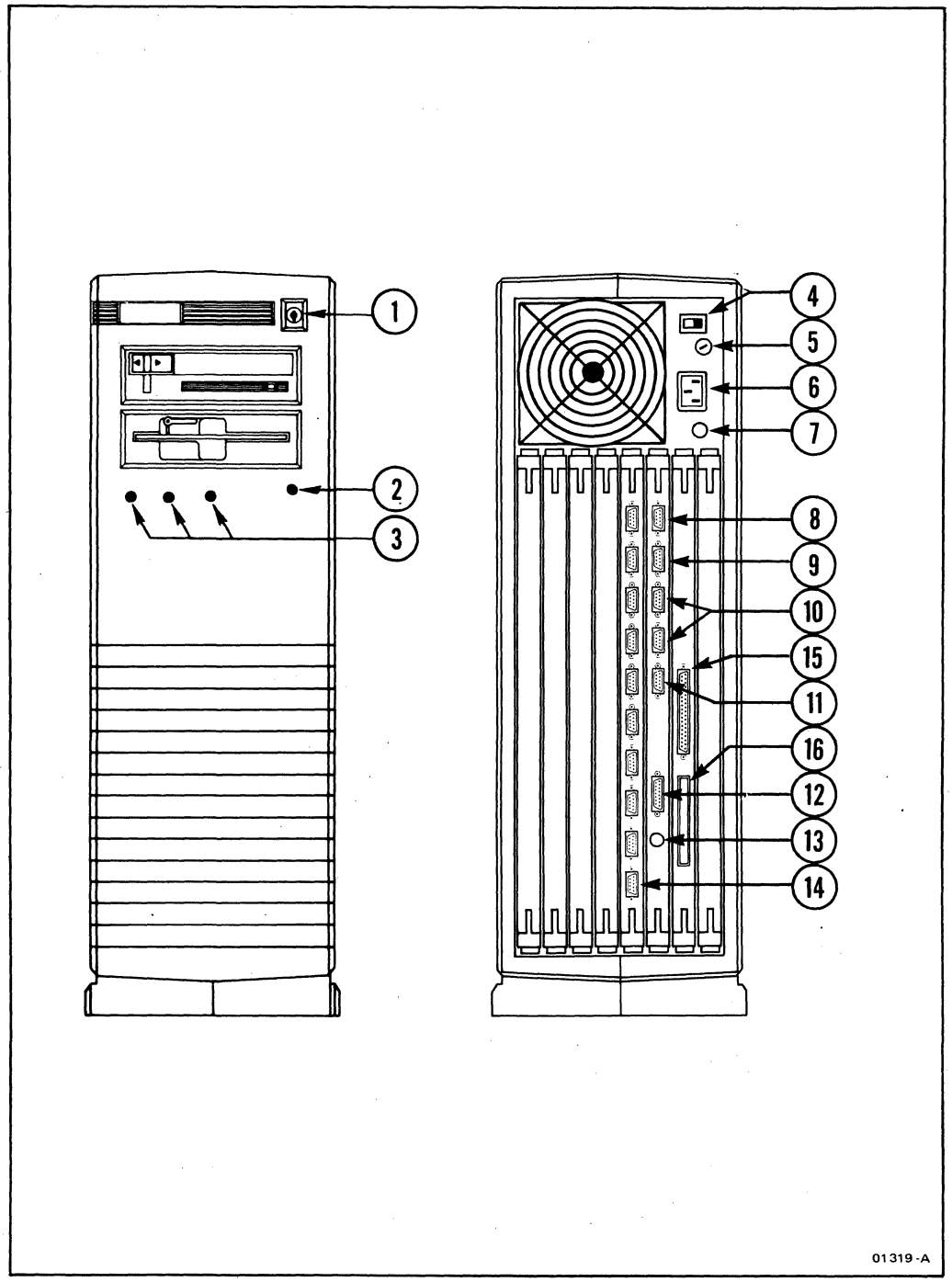

Figure 1-1. Cabinet Controls, Connectors, and Indicators

Cabinet Front Panel

1 **RESET/RUN Switch.** Key-operated switch that resets (boots) the system when turned to RESET and back to RUN. Allows normal system operation when set to RUN. If the key is turned to RESET and removed, the system will remain in the reset condition and will not operate.

2 **POWER Indicator.** Green light-emitting diode (LED) indicator that lights when power is applied to the system (i.e, rear panel POWER switch is in the on position).

3 **HD 1, HD 2, and HD 3.** Yellow LED indicators that light to indicate which hard disk drive is selected.

Cabinet Rear Panel

4 **POWER Switch.** Rocker switch that applies power to the system when placed in the on position (green LED indicator on the front panel is lit). The system will boot when the POWER switch is placed in the off, then on, position while the RESET/RUN switch on the front panel is in the RUN position.

5 **Fuse Holder.** Holder that contains the main power fuse. Refer to the AC Power electrical specifications in Appendix F for the proper fuse ratings.

6 **AC INPUT Connector.** Three-pin AC connector for attaching an AC power cord to the system.

7 **UPS Jack.** Jack for connecting a power fail status signal from an external uninterruptable power source device to the Series 2000 system.

Multidrop Communications Board

8 **Port 0 Connector.** Nine-pin connector for attaching the system console or other asynchronous RS-232 devices to the system.

9 **Port 1 Connector.** Nine-pin connector for attaching asynchronous RS-232 devices or a remote diagnostics modem to the system.

10 **Port 2 and 3 Connectors.** Nine-pin connectors for attaching synchronous/asynchronous RS-232 devices to the system.

11 **Port 4 Connector.** Nine-pin connector for attaching either an asynchronous RS-232 device or WorkNet drop cable.

12 **MULTIDROP Connector.** Fifteen-pin connector for attaching multidropped terminals or TCUs to the system.

13 **FAULT Indicator.** Red light-emitting diode (LED) that lights if the multidrop board does not pass the power-up tests or a nonmaskable interrupt occurs.

SIO Communications Board

14 **Serial I/O Ports.** Connectors 0 through 9 on the communications board provide 10 asynchronous RS-232 ports for connecting terminals or printers to the system. Refer to the SIO communications board operation in Part 2 for details on the serial I/O port capabilities.

File Processor Board

15 **PRINTER Connector.** Connector for attaching a printer with a Centronics-type parallel interface to the system.

16 **SCSI Connector (-002 Version Only).** Connector for attaching SCSI peripherals to the system.

Terminal Cluster Units

Refer to Figure 1-2 for the locations of the terminal cluster unit (TCU) front and rear panel controls, connectors, and indicators.

17 **Port Status Indicators.** Eight yellow light-emitting diode (LED) indicators that indicate the status of each port on the TCU.

18 **POWER Indicator.** Green light-emitting diode (LED) indicator that lights when AC power is applied to the TCU (i.e, POWER switch on the rear panel is placed in the ON position).

19 **RS-232 Ports.** Eight 9-pin ports for connecting RS-232 terminals and printers to the TCU.

20 **STATION ADDRESS Switches.** Five switches (3 through 7) for selecting a unique station address for the TCU.

21 **POWER Switch.** Rocker switch that applies AC power to the TCU when placed in the ON position (green LED indicator on the front panel is lit).

22 **AC INPUT Connector.** Three-pin AC connector for attaching an AC power cord to the TCU.

23 **MULTIDROP Connector.** Fifteen-pin connector for connecting the TCU to the multidrop cable.

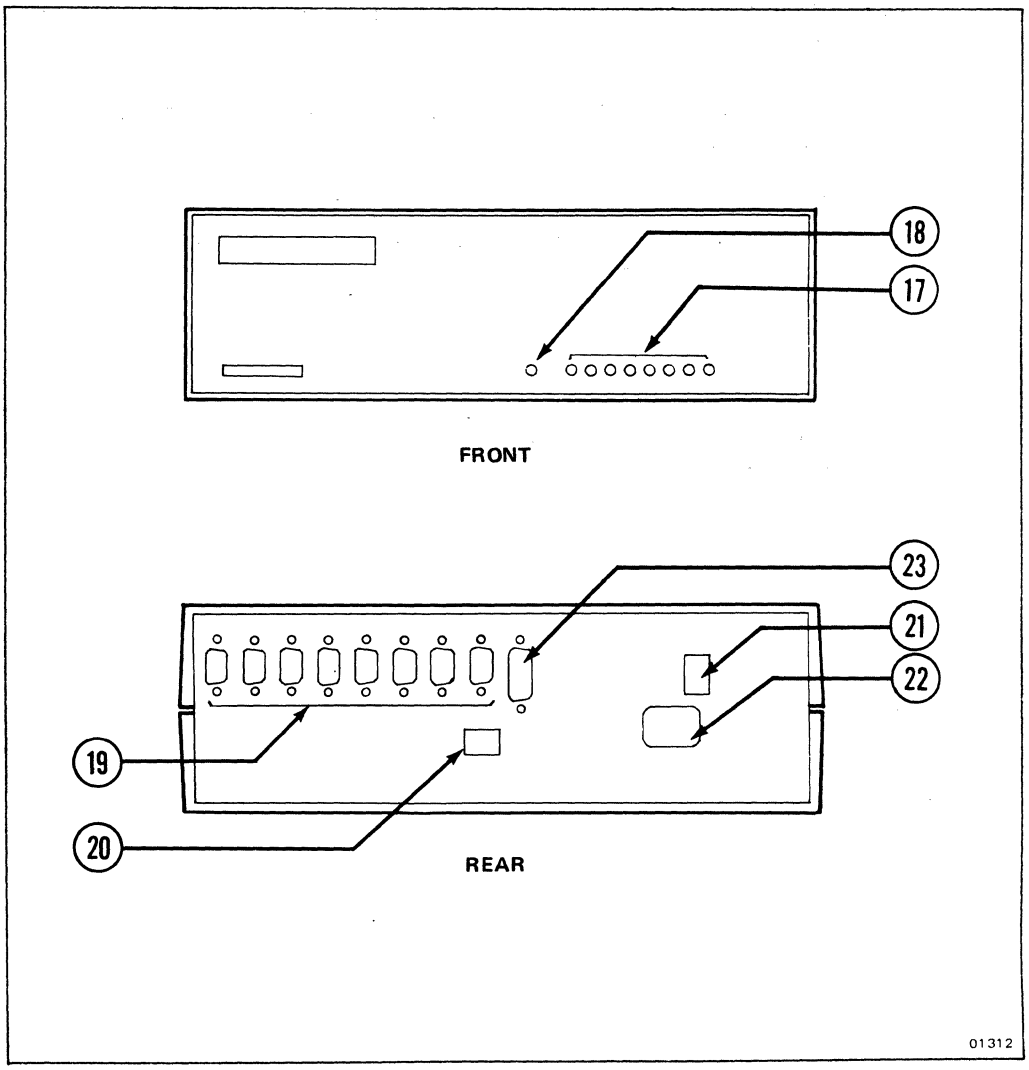

Figure 1-2. Terminal Cluster Unit Controls, Connectors, and Indicators

FIELD-REPLACEABLE UNITS

The following field-replaceable units are available on the Series 2000 (see Figure 1-3):

- central processing unit (CPU) board
- memory board
- multidrop (MDC) or serial input/output (SIO) communications board
- file processor board
- ESDI controller board
- backplane board
- LED board
- main power supply
- tape drive
- floppy disk drive
- hard disk drive
- external terminal cluster unit (TCU)

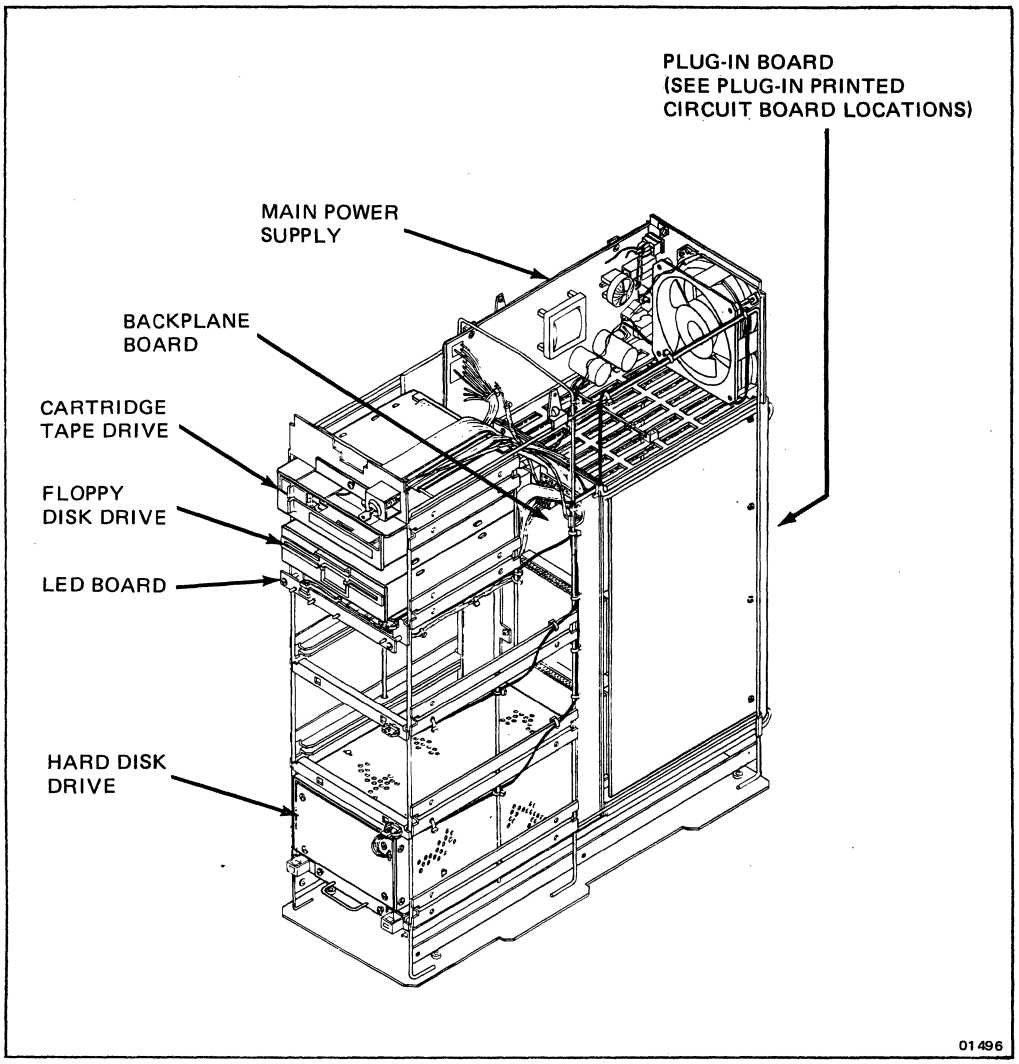

Figure 1-3. Field-Replaceable Units

SYSTEM SOFTWARE

The system software supplied with the Series 2000 consists of the operating system, system-confidence (SDX) tests, and utilities.

Operating System Programs

The Series 2000 is specifically designed for the XENIX operating system which is based on UNIX from AT&T. Altos has added many features to XENIX that support extended development tools, increased performance, and compatibility with existing systems. The XENIX operating system supports menu-driven installation and administrator procedures, and also shared data that allows programs to share a common memory space.

The system hard and floppy disks are controlled by the intelligent file processor board that off-loads much of the processing work from the main CPU. The main CPU uses the address translation logic on the system to improve performance as follows:

- **Scatter Loading.** Loads user programs into non-contiguous 4K byte pages of system memory for more efficient use with less swapping.

- **Context Switching.** When context switching, the per process data area is mapped by loading a table entry instead of copying the data around in memory as in standard XENIX.

- **Dynamic Stack Growth.** Programs do not preallocate stack space, so memory is not wasted with stack space that may never be used.

XENIX also uses disk management techniques to improve performance as follows:

- **Disk-Data Organization.** Altos XENIX supports an implementation of the UNIX file system that maximizes disk throughput, reduces the number of disk accesses, and uses partial blocks to minimize disk fragmentation.

- **Disk Cache.** Disk accesses are reduced by a buffer pool in system memory that acts as a disk cache. The disk cache has a hit ratio of 80% to 95%.

The system I/O ports are controlled by the multidrop and/or SIO communications boards that off-load interrupts and processing from the main CPU. Each communications board is down-loaded with code that handles the asynchronous ports, WorkNet, and any other communication protocols (e.g., SNA, X.25, and bisynchronous communications 3780 and 3270).

Application programs, floppy disks, and cartridge tapes are completely compatible with all Altos 80386 microprocessor-based machines. Also, floppy disks and cartridge tapes are compatible with many other Altos machines, including 8086 microprocessor based XENIX machines.

Diagnostics and Utilities

The system diagnostic executive (SDX) diagnostic tests and utilities are on a floppy disk included with your system. The SDX program performs a series of user system-confidence tests and utilities.

Field-service diagnostics (FDX) tests are available as part of a maintenance package from Altos Customer Support. The FDX tests enable you to locate a faulty field-replaceable unit (FRU) and perform certain utilities.

PLUG-IN PRINTED CIRCUIT BOARD LOCATIONS

The CPU, file processor, and controller boards are dedicated to slots A, G, and H respectively in the back of the Series 2000. The remaining slots, B through F, are electrically identical which allows memory and multidrop or SIO communications boards to be installed in any order in these five slots.

However, software requires that the memory and multidrop and/or SIO communications boards be jumpered according to their function in the system (see jumper description information in **Subsystem Operation** - Chapter 2 and **Jumpers and Switches** - Appendix A).

Thus, if system memory or communications boards are added to the system, Altos recommends that the boards be located as shown in Figure 1-4 to avoid extensive jumper changes on those boards that have already been installed.

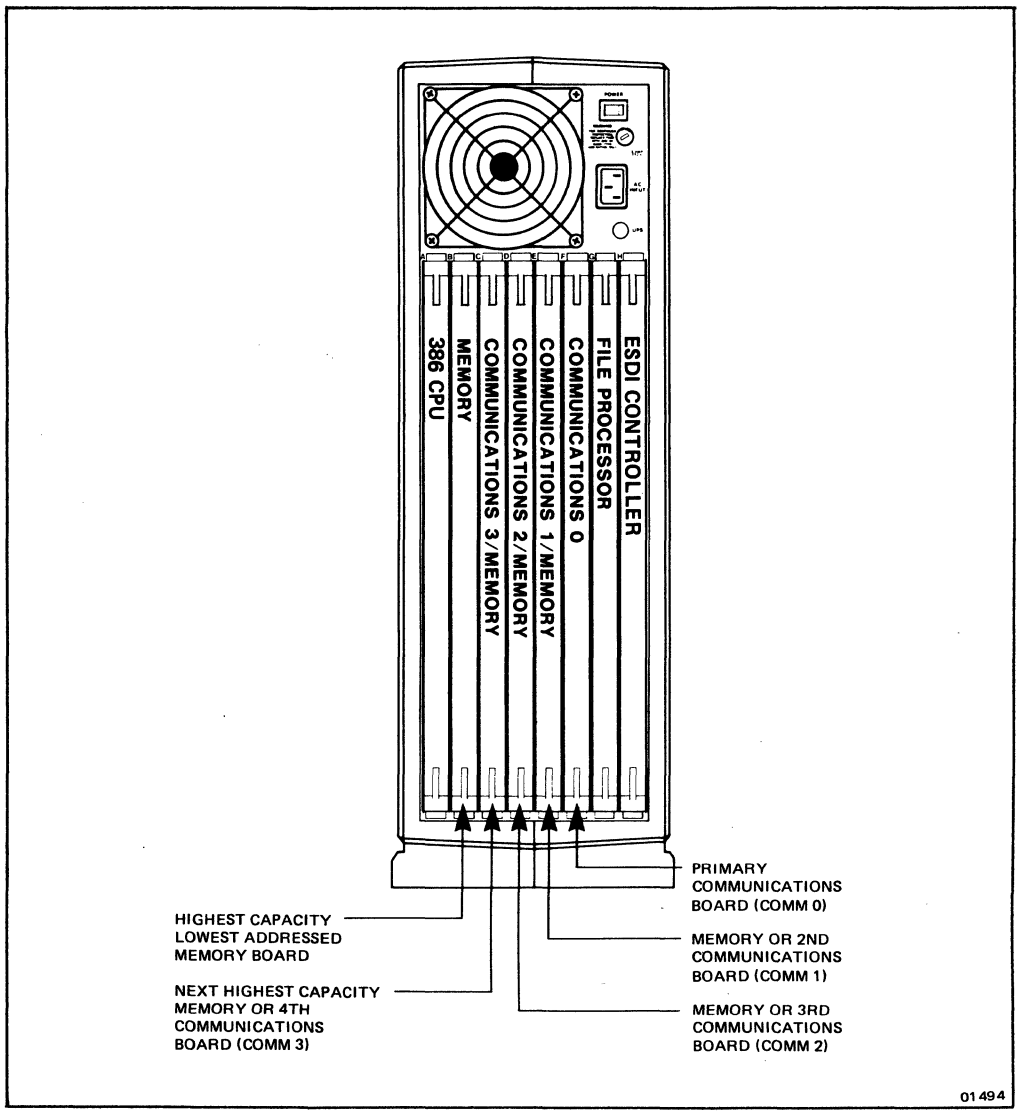

Figure 1-4. Plug-In Board Locations

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Chapter 2
Subsystem Operation

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INTRODUCTION

This chapter is a general block diagram description of the major circuits (subsystems) that comprise the Altos 386 Series 2000 Computer System. The Series 2000 is available with the following major subsystems:

- system bus
- central processing unit (CPU)
- system memory
- multidrop communications
- SIO communications
- file processor
- ESDI controller
- external terminal cluster unit (TCU)

The subsystem hardware is partitioned so that most major functions, except the system bus and terminal cluster unit (TCU), is contained on a single plug-in printed circuit board. The five required boards for the Series 2000 system are the CPU, system memory, communications, file processor, and controller. All of these boards, except the device controller, connect to the 32-bit system bus.

BLOCK DIAGRAM DESCRIPTION

Refer to the system block diagram in Figure 2-1 to help understand the following block diagram description.

System Bus

The Series 2000 system bus is a 32-bit data, 26-bit address bus which is an extension of the IEEE 796 system bus (Multibus I). The

system bus has separate memory and I/O address spaces and can handle asynchronous signal transfers between multiple masters or master and slave. A bus master can perform either single or unlimited system bus transfers. A bus slave decodes addresses and acts upon commands from bus masters. The memory board is the only slave.

Six bus masters (subsystem boards) are supported by prioritized parallel bus arbitration. A bus clock provides bus arbitration and general-purpose timing. Different master-slave subsystems can operate at different clock rates.

The CPU, file processor, and primary communications boards are bus masters which can acquire the system bus through bus exchange logic and generate command, address, and data signals (during writes).

The bus signals are divided into the following signal lines:

- control lines
- address lines
- data lines
- interrupt lines
- bus exchange lines

Central Processing Unit (CPU)

The function of the CPU board is to execute all the system and applications programs. The CPU board uses an 80386 microprocessor, an 80387 80-bit floating-point numeric processor extension, PROM, cache and tag RAM, a calendar clock, and a system bus interface.

The CPU board contains the following four major circuits:

- 80386 microprocessor and 80387 numeric processor
- local bus interface with PROM, RTC, PIC, and CIO
- tag RAM memory interface

- cache RAM memory interface
- 32-bit system bus interface including write buffer

80386 Address Map

The 80386 address map is listed in Table 2-1. The local peripherals include the calendar clock, interrupt controller, CIO (counter with parallel I/O), and PROM.

The address map also contains areas that include the cache memory and tag RAM. The accessibility of these RAMs provides the ability to perform cache diagnostics.

The two remaining areas in the address map are the system bus I/O space and the system bus memory space. When accessing the system bus I/O space, the I/O address is formed by using the lower 16 bits of the 80386 26-bit address. Table 2-2 lists the addresses for the system bus I/O space, Table 2-3 lists the local bus useable addresses, and Table 2-4 lists the real-time clock useable addresses.

Table 2-1. 80386 CPU Address Map

Address	Transfer Length	Description
FFFFFFFF		
F0000000	Word	EPROM
1BFFFFFF		Local I/O (LIO)
180007FF	Word	Debug SCC
18000600		
180005FF	Word	Counter/Timer/I/O (CIO)
18000400		
180003FF	Word	Interrupt Controller (PIC)
18000200		
180001FF	Word	Real Time Clock (RTC)
18000000		
17FFFFFF	Dbl Word	Bus Size RAM (CPIO)
14000000		
13FFFFFF	Byte, Word, Dbl Word	Cache RAM (CIO)
10000000		
0FFFFFFF	Dbl Word	Tag RAM (TIO)
0C000000		
0BFFFFFF	Dbl Word	Cacheable Page
08000000		
07FFFFFF	Byte, Word	System I/O (SMEM*,SBUS)
04000000		
03FFFFFF	Byte, Word, Dbl Word	System Memory (SMEM,SBUS)
00000000		

Table 2-2. System Bus I/O Space (Reserved Locations)

Address	Description
0001h	Communications board 1 (COMM 0) channel attention
0002h	Communications board 2 (COMM 1) channel attention
0003h	Communications board 3 (COMM 2) channel attention
0004h	Communications board 4 (COMM 3) channel attention
000Eh	File processor board channel attention

Table 2-3. Local Bus Useable Addresses

Address	Description
FFFFFFFF	
FFFF8000	EPROM
18000606	Data Port - Debug SCC
18000604	Control Port - Debug SCC
18000406	CIO - Control Port
18000404	CIO - Data A Port
18000402	CIO - Data B Port
18000400	CIO - Data C Port
18000202	PIC - ICW2,ICW3,ICW4,OCW1
18000200	PIC - ICW1,OCW2,OCW3
1800007E	
18000000	RTC - 64 byte locations

Table 2-4. Real-Time Clock Useable Addresses

Address	Description
18000074-1800007F	CPU Firmware
1800006C-18000073	Operating System
1800004C-1800006B	Reserved
1800001C-1800004A	System Users
1800001A	Register D
18000018	Register C
18000016	Register B
18000014	Register A
18000012	Year
18000010	Month
1800000E	Date of Month
1800000C	Day of Week
1800000A	Hours Alarm
18000008	Hours
18000006	Minutes Alarm
18000004	Minutes
18000002	Seconds Alarm
18000000	Seconds

The 80386 microprocessor operates at 16 MHz and executes code out of either PROM, cache memory, or system (RAM) memory. The microprocessor mainly operates from the cache memory which eliminates most wait states.

The local bus on the CPU board transfers address, data, status, and control signals to/from the PROM, calendar clock, interrupt controller, and counter/timer with parallel I/O (CIO).

System Memory

The memory board contains 4M or 8M bytes of 256K x 1 RAM. Memory is organized into 64-bit double-long words. Data transfer is in 8, 16, 24, or 32-bit quantities.

Multidrop Communications

The multidrop communications board supports 30 multidropped terminals and/or asynchronous RS-232 devices interfaced through a terminal cluster unit (TCU) via a 1M bit per second RS-422 interface.

The multidrop communications board also supports multidropped terminals that have integral RS-422 synchronous interfaces. The Altos terminal cluster unit (TCU) converts the high-speed RS-422 synchronous protocol from the multidrop communications board to an asynchronous RS-232 protocol for use by any standard asynchronous RS-232 peripheral (e.g., terminals and printers).

The multidrop communications board also supports WorkNet, two asynchronous/synchronous, and two asynchronous-only RS-232 ports.

The multidrop port (at 1M bit per second) is supported by one dedicated serial channel and associated direct-memory access (DMA) channel.

Altos WorkNet (at 750K or 1.4M bits per second) is supported by a second dedicated serial channel and DMA channel. The two asynchronous/synchronous channels are software configurable to support synchronous protocols.

When running in asynchronous mode, the synchronous/asynchronous ports are intended to support modems or serial printers up to 19,200 baud. The remaining asynchronous-only ports are intended for the system console and a diagnostic modem, or additional serial printer(s).

The multidrop communications board is based upon an Intel 80286 microprocessor running at 6 MHz. The 80286 input/output processor (IOP) can communicate with the system and local buses.

The IOP's interface insures that the local bus is not tied up when the IOP is communicating with the system bus. There is 16K to 32K bytes of initial program load (IPL) PROM and 512K bytes of local RAM. The IPL PROM contains power-up tests, the ability to boot an operating system, and the necessary support for remote diagnostics. Local RAM is used to hold multidrop communications down-load code (from the operating system) and data buffers for all port input/output (I/O).

Four 8530 serial communication controllers (SCCs) support the six I/O channels. Each serial port is DMA-driven to minimize the frequency of interrupts. One-half of an SCC links the multidrop port while another half of an SCC drives the WorkNet port. The other SCCs support the RS-232 synchronous and asynchronous ports and run other communications products. All RS-232 ports can be simultaneously DMA-driven (on both transmit and receive) to increase the performance of communication protocols.

An 8536 counter/timer/parallel I/O (CIO) provides three counter timers for software use, and also provides miscellaneous I/O flags and strobes.

The multidrop communications board interconnects the multidropped terminals and/or the terminal cluster units (TCUs) to the system bus.

Multidrop cabling is electrically similar to and uses the same cables as Altos WorkNet, but with entirely different software protocols which prevents interconnecting WorkNet and multidrop. The maximum trunk length (distance from the computer to the farthest terminal) is approximately 1500 feet extendable by repeaters up to a maximum of 4500 feet. All terminals are polled and the multidrop controller supervises all line usage to eliminate collisions.

The multidrop communications board's on-board firmware has several diagnostic functions that provide power-up confidence tests of all local functions and low-level tests on other parts of the system (on the system bus), including system memory.

SIO Communications

The SIO communications board is an intelligent input/output (I/O) processor that relieves the CPU of all communications functions. The SIO communications board contains an 8086 microprocessor, a system bus interface, a four-channel DMA controller, a local bus controller, 32K to 512K bytes of dynamic RAM, 16 to 256K bytes of PROM, a general-purpose counter/timer, and up to 10 serial ports.

Seven of the serial ports are dedicated to RS-232 asynchronous communications, one is independently software selectable between asynchronous RS-232 and synchronous RS-422 networks, and the

remaining two can support either asynchronous or synchronous RS-232 communications.

Functionally, the SIO communications board is a complete computer with the necessary initial program load (IPL)/diagnostic firmware, RAM, and serial I/O ports.

The SIO communications board's on-board firmware has several diagnostic functions that provide power-up confidence tests of all local functions and low-level tests on other parts of the system (on the system bus), including system memory.

File Processor

The file processor board is an intelligent controller that manages data flow to/from the following:

- floppy disk drive
- cartridge tape drive
- up to three hard disk drives
- Centronics-type parallel printer interface
- additional drives through the small computer system interface (SCSI) channel

The file processor board contains the following circuit elements:

- 8086 microprocessor
- four-channel DMA controller
- system bus interface
- local bus controller
- 128K bytes of dynamic RAM
- 16K bytes to 32K bytes of PROM
- counter/timer

- disk and printer interface
- SCSI controller

ESDI Controller

The Series 2000 uses an enhanced small device interface (ESDI) controller board. The controller board contains three independent controllers for streaming tape, floppy disk, and hard disk drives. All controllers receive commands from the file processor board.

The tape drive controller supports Altos cartridge tape drives with QIC-36 interfaces, and uses the QIC-24 format to input data on the tape.

The floppy disk controller supports one internal, dual-speed, double-density, double-sided, 96 track per inch (TPI), floppy disk drive.

The hard disk controller on the ESDI controller board can support three internal ESDI hard disk drives. The hard disk controller can accommodate serial data rates to 10M bits per second and is capable of seek-overlap operation when multiple devices are used.

Terminal Cluster Unit

The terminal cluster unit (TCU) is based upon multiple Intel 8044 microcontrollers or remote universal peripheral interfaces (RUPIs) which are single-chip microcontrollers operating at 9.83 MHz. The RUPI contains an 8051 microprocessor core, two counter timers, an interrupt controller, a high-speed DMA controller, 192 bytes of dual-ported RAM, 4K of mask ROM, and a serial interface unit (SIU) capable of supporting synchronous communications. The 8051 CPU and SIU can run concurrently.

There is one 8044 dedicated to driving each RS-232 serial port. The 8044's SIU is designed to perform serial communications to the multidrop communications board with little CPU involvement. Much of the synchronous data link control (SDLC) protocol handling is implemented on-chip. The SIU transmits data at 983K bits per second, and can receive at rates up to 2M bits per second (determined by the transmit rate of the multidrop communications

board - typically 1M bits per second). The line protocol is carrier-sense, multiple access (CSMA), polled.

A single-channel UART (Motorola MC2661 enhanced programmable communications interface - EPCI) is used to provide communications between the RUPI and the RS-232 serial device. All RS-232 communications parameters (i.e., baud rate, number of stop bits, handshaking, etc.) are under software control via the RUPI.

A switch on the TCU sets the station identification addresses, which allows the multidrop communications board to uniquely address each RS-232 serial device.

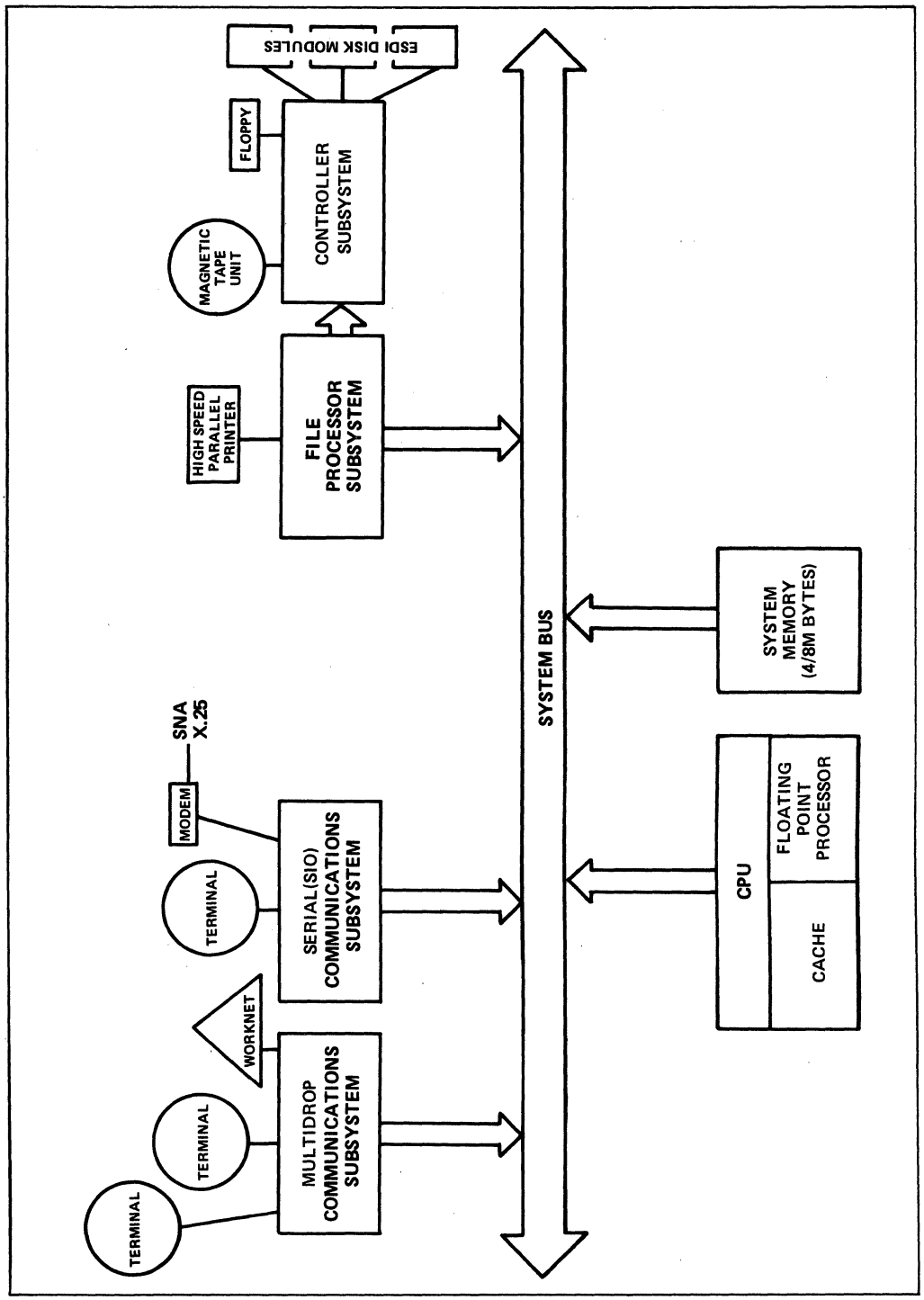

Figure 2-1. Series 2000 System Block Diagram

How to Use This Section

This maintenance section provides troubleshooting, removal/ replacement, and preventive maintenance information. Preventive maintenance consists of cleaning the component parts of the system. Also included are instructions for shipping field-replaceable units to the factory or service center for repair or replacement.

Before you begin to troubleshoot, look at the following trouble-shooting guide to help you determine which of the troubleshooting procedures in Chapters 3 through 5 will quickly locate the problem.

Troubleshooting Procedure Guide

Trouble Symptom	Procedure
System does not appear to have power	1. Use **Power-Up Checks** - Chapter 3
Power-up cycle does not complete or ther is an error message	1. Use **Power-Up Checks** - Chapter 3 2. Use **Monitor Debugger** - Chapter 5
Power-up cycle completes but system does not boot	1. Use **Power-Up Checks** - Chapter 3 2. Use **Floppy-Based Diagnostics** - Chapter 4 3. Use **Monitor Debugger** - Chapter 5
Power-up and boot are ok but processing fails (operating system error message	1. Refer to Operating System manual to determine if failure is software or hardware related. If hardware related: 2. Use **Floppy-Based Diagnostics** - Chapter 4 3. Use **Monitor Debugger** - Chapter 5

Chapter 3
Power-Up Checks

(BLANK)

INTRODUCTION

This chapter contains power-up troubleshooting information for locating a faulty field-replaceable unit (FRU) on the Altos 386 Series 2000 Computer System. However, if problems persist after performing the power-up checks described in this chapter, refer to **Floppy-Based Diagnostics** - Chapter 4 for additional test information.

PRELIMINARY TROUBLE ANALYSIS

If the system fails to power-up or boot, use Table 3-1 to help determine the cause of the problem. Most of these preliminary checks do not require qualified service personnel.

CAUTION

Before attempting to troubleshoot, be sure that the main power supply is set for the proper AC line voltage. (Refer to 115/230 VAC Conversion - Appendix F for the main power supply AC conversion instructions.)

Table 3-1. Preliminary Trouble Analysis

Symptom	Probable Cause	Corrective Action
1. No display appears on system console. System seems dead.	a. Reset/Run switch is in Reset	Set Reset/Run switch to Run
	b. Screen has cycled off	Press Retn key
	c. Brightness or contrast too low	Adjust console terminal brightness and contrast controls
	d. Terminal cable loose or defective	Check/replace cable from port 0 of primary communications board (COMM 0)
	e. No AC power from receptacle	Check for AC to receptacle. Check/replace AC receptacle
	f. Power cord loose or defective	Check/replace power cord
	g. Fuse blown	Check/replace fuse (replace with proper value)
	h. Faulty power supply	Replace power supply
2. Fuse blows repeatedly	a. Short circuit in system	Remove all drives and plug-in boards. Replace fuse and apply power - see cause (b)
	b. Faulty main power supply	Check/replace main power supply

Table 3-1. Preliminary Trouble Analysis (Cont.)

Symptom	Probable Cause	Corrective Action
2. Fuse blows repeatedly (Cont.)	c. Faulty plug-in board subsystem	Install one plug-in board. Replace fuse and apply power. Repeat for each plug-in board until faulty board is found. Replace faulty board
3. Display appears but no response from keyboard	a. System "hung"	Reset system
	b. Terminal or system trouble	Check terminal by plugging into another system, or check other terminals on the system

WARNING

Hazardous voltages are present in the power supply. Use extreme caution when measuring voltages.

NOTE

The power supply is a switching type. Check under load to ensure accurate results.

	c. Power supply DC voltages out of tolerance	Check power supply voltages with a digital voltmeter. Refer to Table 3-2 for power supply DC output voltages)

Table 3-2. Power Supply DC Voltages

Voltage*	Measured At	Range
+5	JB, Pin 4	+5.0 to +5.2
+12	JB, Pin 1	+11.4 to +12.6
-12	JA, Pin 9	-11.4 to +12.6
Gnd	JB, Pin 2	

* Measure the power supply output voltages with a precision DC voltmeter. Connectors JA and JB are located along the top of the backplane board. Make the measurements with the tape and floppy drives connected.

If the power supply output voltages are out of tolerance, return the power supply to the factory for repair or replacement. Refer to **Removal/Replacement** - Chapter 6 for specific removal and replacement procedures.

MONITOR COMMUNICATION PROTOCOL

Monitor communication between the CPU, communications, and file processor firmware is accomplished through groups of parameter blocks in the system memory. All communication requires CPU intervention except during power-up. Thus, no direct communication between controllers is allowed.

For example, if the file processor needs to print a message, it must send the print command to the CPU board, which will then route the request to the communications board for actual display.

During power-up time, the primary communications board firmware assigns each controller (e.g., file processor, up to three other communications boards, and the CPU board) a 320 byte space in system memory (64 bytes for the parameter block and 256 bytes for the buffer) to be used as the parameter block and message buffer.

Subsequently, all communications are done on a one-to-one basis between the CPU and file processor, or between the CPU and the individual communications boards.

SYSTEM POWER-UP SEQUENCE

The power-up tests use the ROM-based diagnostic tests contained on the CPU, communications, and file processor boards. The power-up tests are always performed when power is applied or the system is reset. Refer to Figure 3-1 for a block diagram of the power-up test sequence. These tests check the hardware configuration on each board, identify any missing or failed assemblies, and then confirm communication with the system as follows:

- communications tests check local RAM and PROM, I/O integrated circuits, DMA controller, interrupts, system bus, and initialize memory
- CPU tests check the PROM, cache RAM, counter/input/output (CIO), tag RAM, clock, floating-point processor, interrupts, and system bus o file-processor tests check the local RAM and PROM, interval timer, system bus, DMA controller, and storage device controllers

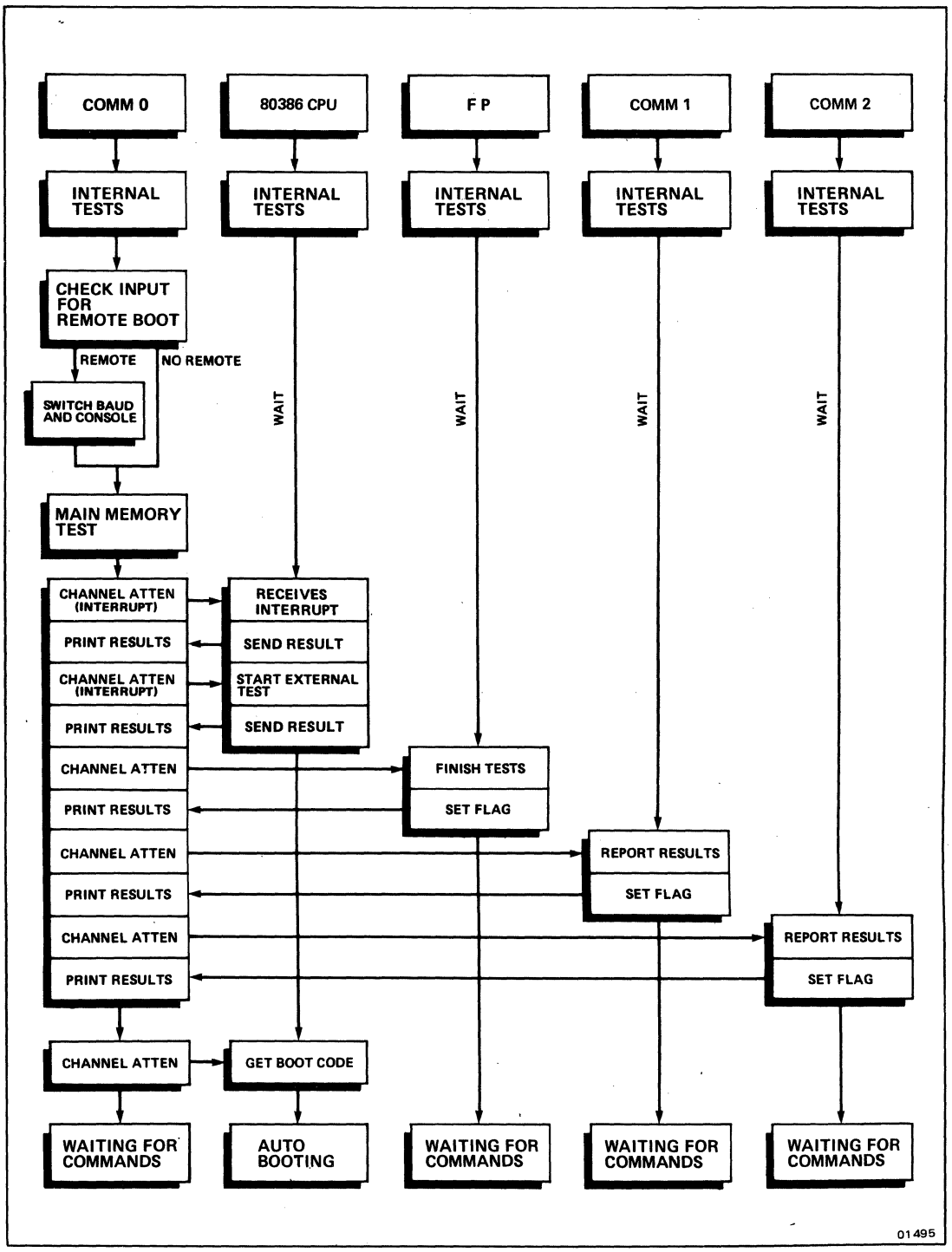

Figure 3-1. System Power-Up Test Sequence

During power-up, the primary communications board firmware proceeds in the following sequence:

1. After internal verification, the primary communications board firmware sends a COMMUNICATIONS BOARD POWER-UP TESTS message to port 0 (main console).

2. After internal verification, the primary communications board checks for remote diagnostics.

3. After internal verification, the primary communications board tests the system memory.

4. After the internal and external tests are completed, the primary communications board sets up a firmware protocol block and sends a channel attention to the CPU board. The primary communications board will timeout if the CPU does not respond in a few seconds.

5. After receiving acknowledgement from the CPU board, the primary communications board displays its power-up test results on the main console (port 0).

6. The primary communications board performs the same test requests for the file processor board. If there is a file processor error, a corresponding error message is displayed.

7. Other communications (multidrop and/or SIO) boards are checked for availability.

8. The auto boot from the hard disk (highest logical priority device) is performed, unless the user presses a key to interrupt the process.

9. If the boot operation is successful, control is transferred. Otherwise, an error message is displayed with a new menu to allow the user to either boot from a particular device or enter the debugger routine.

10. If a floppy disk boot is requested, the CPU board tries a slow-speed check for dual-speed floppy disk drives. If this fails, then a high-speed check is attempted. If both of these checks fail, then the boot menu is displayed.

POWER-UP TESTS

The system firmware consists of the system (or resident) monitor program which is a collection of routines that remain permanently in programmable read-only memory (PROM) on the CPU board. The function of the monitor program is to validate the system and provide down-load and disk-boot capability which permits the user to load operating systems and programs into the system memory.

The monitor program consists of three routines: power-up, disk-boot, and monitor debugger (see **Monitor Debugger** - Chapter 5). The power-up tests perform the necessary initialization sequences required by the hardware and identify all major hardware components functioning properly upon power-up or reset.

The disk-boot routine allows the operating system or test programs to be loaded into system memory from a particular device. When this boot operation is successful, the control is transferred to the newly loaded code.

The Series 2000 contains a minimum of five printed circuit boards. Three of these boards have microprocessors: the central processing unit (CPU), file processor, and communications (multidrop and/or SIO) boards. Each of the three microprocessor-based boards performs dedicated functions with the main processing tasks executed by the CPU board.

The terminal and network communications are performed by the communications board(s) while the file processor board handles the storage device support. Each of these boards has its own firmware support, which provides power-up verification, hardware initialization, and user monitor call support in a local environment. In addition, the communications board firmware coordinates the system-level power-up sequences as well as monitoring the overall communication between all the firmware at power-up time.

Communications (Multidrop or SIO) Power-Up Tests

Upon power-up, the communications firmware performs the following power-up confidence tests:

1. **Checksum the PROMs.** The PROMs are summed separately to determine which one(s) to replace. A failure of the checksums is considered a major failure because the integrity of the PROMs is in doubt. No other tests can be trusted since they may pass from unknown changes in the firmware. If the communications CPU starts up properly, the red LED turns off.

2. **Local Bus Data Ripple.** The main RAM is on a 16-bit bus. The first word is used to test the data lines. A 1 bit is rippled through the data lines, then a 0 bit is rippled through.

3. **Local Bus Content March.** The local RAM is tested with two patterns, 5555 and AAAA. This test simply marches through RAM one word at a time. After each location is tested, it is cleared with a 0.

4. **CIO.** The internal registers are loaded and checked for valid data.

5. **SCC0.** The internal registers are loaded and checked for valid data.

6. **SCC1.** The internal registers are loaded and checked for valid data.

7. **SCC2.** The internal registers are loaded and checked for valid data.

8. **SCC3.** The internal registers are loaded and checked for valid data.

9. **DMA Controller.** The internal registers are loaded and checked for valid data. Memory-to-memory transfer is executed which tests the ADMA functions and interrupts.

10. **System Memory.** The system memory is sized in 64K byte blocks. Then each block is tested with the standard patterns of 5555 and AAAA. After a location is tested it is cleared.

CPU Power-Up Sequence

The CPU monitor program performs the following steps upon power-up or reset:

1. Save the 80386 CPU self-test result.
2. Load the PROM-based global descriptor table address into GDTR and switch to protected mode.
3. Make a intersegment jump to execute in 32-bit mode.
4. Run tests 1 through 8.
5. Set up global descriptor table and interrupt descriptor table in cache set 0 and change GDTR and IDTR accordingly.
6. Run tests 9 through 23.
7. Wait for the first valid interrupt from SIO/multidrop board.
8. Place internal power-up test result in system memory and issue the first channel attention to SIO/multidrop board for acknowledgment.
9. Wait for the second valid interrupt from SIO/ multidrop board.
10. Load global descriptor table and interrupt descriptor table into system memory. See Note 1.
11. Change registers GDTR and IDTR.
12. Perform tests 24 through 31.
13. Place external power-up test result in system memory and issue the second channel attention to SIO/multidrop board to signify the completion of tests.
14. Wait for the third valid interrupt from SIO/multidrop board.

15a. Get the boot number and system configuration code. Set up global descriptor table and interrupt descriptor table in cache set 0 and change GDTR and IDTR accordingly. Then, perform the boot from either highest logical priority device, user-requested device, or enter the debugger. See Note 2.

15b. Wait for the first double word containing a nonzero address and execute that address.

NOTE 1: Step 10 only applies to the CPU that is placed in slot A.

NOTE 2: Step 15a applies to the CPU that is placed in slot A. Step 15b applies to the CPU that is not placed in slot A.

The SIO or multidrop board sets up the communication block prior to sending the interrupt request to the target CPU. The normal CPU power-up sequence as briefly described above is accomplished in more detail as follows.

Upon completion of the internal tests, all the CPUs are waiting for the first valid channel attention before reporting their results. Then, the CPUs are each given another channel attention to start the external tests. Only if a CPU sees a valid ID for its respective slot will it respond to any request for status. Thus, when the CPUs detect a valid channel attention, the CPUs place their results in the communication block and send back a channel attention to the SIO/multidrop board.

Note that the CPUs are not given commands because they only respond to a sequence. When the SIO/multidrop board gives out the boot channel attention (ID=7562h), all the CPUs will respond. However, only the master CPU (in slot A) will boot while the others (if applicable) wait until the operating system is loaded. In addition, only the master CPU is allowed to actually give commands to the file processor and SIO/multidrop boards. The slave CPU will wait for the first double word containing a nonzero address and then jump to that address.

CPU Monitor Address Map

Table 3-3 provides a map of the monitor addresses.

Table 3-3. Monitor Address Map

Address	Description
00000000 - 03FFFFFF	System bus memory space
10000000 - 100001FF	Monitor global descriptor table
10000200 - 100003FF	Monitor interrupt descriptor table
10000400 - 10000FFF	Monitor data area
10001000 - 100017FF	Monitor stack area
0007F000 - 0007F03F	SIO-1 parameter block
0007F040 - 0007F13F	SIO-1 message block
0007F140 - 0007F17F	SIO-2 parameter block
0007F180 - 0007F27F	SIO-2 message block
0007F280 - 0007F2BF	SIO-3 parameter block
0007F2C0 - 0007F3BF	SIO-3 message block
0007F3C0 - 0007F3FF	SIO-4 parameter block
0007F400 - 0007F4FF	SIO-4 message block
0007F500 - 0007F53F	File processor parameter block
0007F540 - 0007FFFF	File processor message buffer
04000000 - 0400FFFF	System I/O
08000000 - 0800FFFF	Cacheable page RAM
14000000 - 17FFFFFF	Bus size RAM
0C000000 - 0C003FFF	Tag RAM
10000000 - 10003FFF	Cache RAM (set 0)
10004000 - 10007FFF	Cache RAM (set 1)
18000000 - 1800007F	MC146818A (RTC)
18000200 - 18000202	8259 (PIC)
18000400 - 18000406	Z8536 (CIO)
FFFF8000- FFFFFFFF	EPROM

Global Descriptors

Table 3-4 provides a list of the global descriptors.

Table 3-4. Global Descriptors

Selector	Descriptor	Address
0000	Null descriptor	Not defined
0008	Global descriptor table	10000000 - 100001FF
0010	Interrupt descriptor table	10000200 - 100003FF
0018	Monitor code descriptor	FFFF8000 - FFFFFFFF
0020	Monitor data descriptor	10000400 - 10000FFF
0028	Monitor stack descriptor	10001000 - 100017FF
0030	Cache RAM descriptor	10000000 - 10007FFF
0038	System I/O descriptor	04000000 - 0400FFFF
0040	Common data descriptor	0007D400 - 0007DFFF
0048	Tag descriptor	0C000000 - 0C0008FF
0050	Local I/O descriptor	18000000 - 1800FFFF
0058	Cache page RAM descriptor	08000000 - 17FFFFFF
0060	Memory data segment 00	00000000 - 0000FFFF
0068	Memory code segment 00	00000000 - 0000FFFF
0070	Memory data segment 01	00010000 - 0001FFFF
0078	Memory code segment 01	00010000 - 0001FFFF
0080	Memory data segment 02	00020000 - 0002FFFF
0088	Memory code segment 02	00020000 - 0002FFFF
0090	Memory data segment 03	00030000 - 0003FFFF
0098	Memory code segment 03	00030000 - 0003FFFF
00A0	Memory data segment 04	00040000 - 0004FFFF
00A8	Memory code segment 04	00040000 - 0004FFFF
00B0	Memory data segment 05	00050000 - 0005FFFF
00B8	Memory code segment 05	00050000 - 0005FFFF
00C0	Memory data segment 06	00060000 - 0006FFFF
00C8	Memory code segment 06	00060000 - 0006FFFF
00D0	Memory data segment 07	00070000 - 0007FFFF
00D8	Memory code segment 07	00070000 - 0007FFFF
00E0	Memory data segment 08	00080000 - 0008FFFF
00E8	Memory code segment 08	00080000 - 0008FFFF
00F0	Memory data segment 09	00090000 - 0009FFFF
00F8	Memory code segment 09	00090000 - 0009FFFF
0100	Memory data segment 0A	000A0000 - 000AFFFF
0108	Memory code segment 0A	000A0000 - 000AFFFF

Table 3-4. Global Descriptors (Cont.)

Selector	Descriptor	Address
0110	Memory data segment 0B	000B0000 - 000BFFFF
0118	Memory code segment 0B	000B0000 - 000BFFFF
0120	Memory data segment 0C	000C0000 - 000CFFFF
0128	Memory code segment 0C	000C0000 - 000CFFFF
0130	Memory data segment 0D	000D0000 - 000DFFFF
0138	Memory code segment 0D	000D0000 - 000DFFFF
0140	Memory data segment 0E	000E0000 - 000EFFFF
0148	Memory code segment 0E	000E0000 - 000EFFFF
0150	Memory data segment 0F	000F0000 - 000FFFFF
0158	Memory code segment 0F	000F0000 - 000FFFFF
0160	Monitor variable data segment	Variable
0168	Monitor variable code segment	Variable
0170	Monitor variable data segment	Variable
0178	Monitor variable code segment	Variable
0180	Four gigabyte data segment	00000000 - FFFFFFFF
0188	Four gigabyte code segment	00000000 - FFFFFFFF
	Not initialized	
01F8	Not initialized	

Universal Parameter Block

Table 3-5 describes the universal parameter block.

Table 3-5. Universal Parameter Block Description

Relative Byte Address (Decimal)	Description
00	Device number (low byte)
01	Device number (high byte)
02	Command (low byte)
03	Command (high byte)
04	General status (low byte)
05	General status (high byte)
06	Device dependent status 0
07	Device dependent status 1
08	Device dependent status 2
09	Device dependent status 3
10	Buffer addr. (low byte)
11	Buffer addr. (high byte)
12	Buffer addr. (middle high byte)
13	Buffer addr. (most significant byte)
14	Device specific parameters
15	Device specific parameters
16	Device specific parameters
17	Device specific parameters
18	Device specific parameters
19	Device specific parameters
20	Device specific parameters
21	Device specific parameters
22	Device specific parameters
23	Device specific parameters
24	Device specific parameters
25	Device specific parameters
26	Device specific parameters
27	Device specific parameters
28	Device specific parameters
29	Device specific parameters
30	Device specific parameters

CPU Power-Up Tests

The CPU power-up test sequence starts with a series of tests that validate the system. Tests 1 through 23 are done on the CPU board while the rest of the tests access system memory and are performed after the first valid channel attention from the communications board (SIO or multidrop) is received.

At the beginning of each test, the monitor outputs a status code to CIO port B to indicate which test is in progress. If an error is detected during a test, the monitor tests for a loop bit set (CIO-PA2=0) to loop on error. In addition, the monitor will output a test message to an external diagnostic port if it is installed.

The CPU power-up tests are executed as follows:

1. **80386 CPU Self Test.** The 80386 is forced into self test by the hardware after the reset signal becomes inactive. The self test checks the function of the control ROM and most of the non-random logic of the ROM. If the ROM passes the self test, the contents of the EAX register are zero.

2. **PROM Checksum.** The PROMs are summed separately in order to indicate which one is bad. A failure of the checksum is considered a major failure because the integrity of the PROMs is in doubt.

3. **Cache RAM Set 0 Data Ripple.** The cache RAM set 0 is located from 10000000 to 10003FFFh. The first two double words (8 bytes) are used to test the data lines. A one (1) is rippled through the data lines then a zero (0) is rippled through.

4. **Cache RAM Set 1 Data Ripple.** The cache RAM set 1 is located from 10004000 to 10007FFFh. The first two double words (8 bytes) are used to test the data lines. A one (1) is rippled through the data lines then a zero (0) is rippled through.

5. **Cache RAM Set 0 Address Ripple.** Forty eight locations of the cache RAM set 0 are loaded with different background patterns. Then each selected location is checked by reading out the written pattern, writing the complement of data pattern and reading back again to verify.

6. **Cache RAM Set 1 Address Ripple.** Forty eight locations of the cache RAM set 1 are loaded with different background patterns. Then each selected location is checked by reading out the written pattern, writing the complement of data pattern and reading back again to verify.

7. **Cache RAM Set 0 Content March.** The cache RAM set 0 is tested with two patterns, 55 and AAh. This test first writes the whole set of cache with 55, two words at , a time. Then it reads the data and writes its complement, one byte at a time. This test leaves data pattern AAh in the cache RAM.

8. **Cache RAM Set 1 Content March.** The cache RAM set 1 is tested with two patterns, 55 and AAh. This test first writes the whole set of cache with 55, two words at a time. Then it reads the data and writes its complement, one byte at a time. This test leaves data pattern AAh in the cache RAM.

9. **Bus-Size RAM Data Ripple.** The bus-size RAM is located from 14000000 to 17FFFFFFh. The first double words (4 bytes) are used to test the data lines. Only two data lines need to be tested. Four different patterns (bit 29, 28 = 00,01,10,11) are used in this test.

10. **Bus-Size RAM Address Ripple.** This test checks the integrity of the bus-size RAM address bus. There are twelve address lines to test. A one (1) is rippled through the address line lines then a zero (0) is rippled through.

11. **Bus-Size RAM Content Test.** The bus size ram is tested with two patterns (bit 29, 28 = 10, 01). This test first writes the whole RAM with 10b. Then it reads the data and writes its complement.

12. **Z8536 (CIO) Test.** This test first reads back the contents of two internal registers which have been initialized upon power up. Then the counter/timer 1 time constant register (MSB) is tested by rippling a one (1) through the data lines.

Finally, all three timers are set up to run independently and the command/status registers are read to verify that all three counters are exhausted.

13. MC146818A (RTC) Data Ripple. This test first checks to see if the realtime clock contains the initialized pattern. If so, it indicates that the MC146818A IC has been tested and initialized before. Tests 13 through 15A are skipped. Otherwise, the data ripple test is then executed. The real-time clock is located from 18000000 to 1800007Fh.

There are eight data lines to test. The internal RAM location 0Eh is used to test the data lines. A one (1) is rippled through the data lines, then a zero (0) is rippled through.

14. MC146818A (RTC) Address Ripple. This test first writes to seven selected locations using the address as the background pattern. Then each location is read back to verify.

15A. MC146818A (RTC) Content. There are sixty-two read/write locations in the MC146818A ICs and all of them are tested with two patterns, 55 and AAh, one byte at a time.

15B. MC146818A (RTC) Counter. This test first writes a zero to the SET bit (bit 7 of Register B of MC146818A) to enable the counter and then checks for the end of the update cycle. At the end of the test, the last three bytes of ram are written with 59h, 52h and 19h to indicate that the clock chip has been tested and initialized. Hence these three locations are reserved by the monitor.

16. 80387 (Numerical Processor) Test. The 80387 is initialized and the status is read. The status (low byte) will be zero if the 80387 is in its socket and functioning. If the status is good, two binary numbers in cache RAM are multiplied, and the result placed in another location. The result is then checked for the correct value.

17. Cacheable Page RAM Data Ripple Test. The cacheable page RAM is located from 08000000 to 0800FFFFh. The first double words (4 bytes) are used to test the data lines. There are two data lines (TD30 and TD31) to test. Four different pattern (bit 31, 30 = 00, 01, 10, 11) are used in this test.

18. Cacheable Page RAM Address Ripple Test. This test checks the integrity of the cacheable page RAM address bus. There are fourteen address lines to test. A one (1) is rippled through the address lines then a zero (0) is rippled through.

19. Cacheable Page RAM Content Test. The cacheable page RAM is tested with two patterns (bit 31, 30 = 01, 10). The test first writes the whole RAM with pattern 01. Then the data is read and its complement is written. Finally, the whole RAM is written with pattern 11 to leave all ones (1s) in the cacheable page RAM.

20. Tag RAM Data Ripple. The tag RAM is located in address space 0C000000 to 0C003FFFh. There are twentyeight data lines to test. The first double word location is used to test the data lines. A one (1) is rippled through the data lines, then a zero (0) is rippled through.

21. Tag RAM Address Ripple. This test checks the integrity of the tag RAM address bus. If the block size of cache is configured to 4 bytes, there are twelve address lines to test. Otherwise, the block size of cache is configured to 8 bytes and there are eleven address lines to test. A one (1) is rippled through the address lines then a zero (0) is rippled through.

22. Tag RAM Content March. The tag RAM is tested with two patterns, 55 and AAh. For a 4 byte block size of the cache, there are 4K locations to test. Otherwise, there are only 2K locations to test. This test first writes the whole RAM with 55h, two words at a time. Then the data is read and its complement is written.

23. 8259A (PIC) Test. The PIC is set up for fully nested, no buffer, auto end of interrupt (EOI), 8086 mode of operation. Then OCW1 is written and read back nine times to test if the 8259A IC is there or not. Then IR0 is tested through the CIO timer.

24. INT5* and INT6* Test. The INT5* and INT6* are tested separately through the CIO port B and PIC. If interrupts IR6 and IR7 are detected, the test passes.

25. Cache Write Miss Test. Both tag sets are first made invalid. Then, both cache sets are set to zero. Two 16K byte blocks of system memory are written to with FFh while both sets of cache are enabled. Finally, the cache is disabled and checked to see if the contents remain unchanged. The cache should never be updated in this test.

26. Cache Read Miss Test. Four 16K blocks of the third 64K segment of system memory are written with different patterns while cache is disabled. The following test sequence is performed:

1. Cache set 0 is enabled and the first 16K block is read.

2. Cache set 0 is disabled and checked to see if it contains the proper data and that tag 0 is updated to the correct value.

3. Cache set 0 is disabled and cache set 1 is enabled and the second 16K block is read.

4. Cache set 1 is disabled and verified for the correct data and tag 1 is updated accordingly.

5. Both cache sets are enabled and the third 16K block is read.

6. Both cache sets are disabled and checked to see if cache set 0 and tag set 0 contain the proper contents. The tag set 0 should be updated and the tag set 1 should remain unchanged.

7. Both cache sets are then enabled and the fourth 16K block is read.

8. Both cache sets are disabled and verified to determine that cache set 1 contains the proper data and that tag set 1 is updated and tag set 0 is unchanged.

27. Cache Write Hit Test. All the tags are valid from the above test. Both cache sets are enabled and the third and fourth 16K block of the third 64K segment of system memory are written with zero (0). Then, the cache is disabled and verified to determine that the contents of both cache sets are zero.

28. Cache Read Hit Test. All the tags are valid from the above test and the cache is disabled. The contents of the cache is zero (0). The contents of the third and fourth 16K block of the third 64K segment of system memory are also zero (0).

Then, both cache sets are loaded with FFh. Cache is enabled and the third and fourth 16K block of the third 64K segment of system memory are read to verify that the contents are FFh.

29. Force Cache-Read Miss Test. All the tags are valid from the above test. The contents of cache are FFh. The cache is enabled and the CMISS* bit is set to 0. Then, the third and fourth 16K block of the third 64K segment of system memory is read to verify that the contents are zero (0).

30. Tag Invalidation Test. The tags are made valid from the above test. The cache is enabled and the TSTBIT is set to simulate a write from other bus masters. The third and fourth 16K block of the third 64K segment of system memory is written with FFh. Then, the tags are checked to see if the valid bits are set to invalid.

31. Cache Execution Test. First, both tags are made invalid and the following test sequence is performed:

1. The cache is enabled and the first 16K block of the third 64K segment of system memory is read.
2. Both cache sets are disabled.
3. Cache set 0 is loaded with 'inc edx' instructions and the last 7th byte in the block is loaded with intersegment 'jmp' instructions.
4. The first 16K block of the third 64k segment of system memory is written with zero (0).
5. Both cache sets are enabled.
6. A 'jmp' is made to the beginning of this 16K block and executed.
7. The edx register is checked for the correct value.
8. Cache set 0 is disabled and cache set 1 is enabled.
9. The second 16K block of the third 64K segment of system memory is read.
10. Both cache sets are disabled.
11. Cache set 1 is loaded with 'inc ebx' instructions and the last 7th byte of the block is loaded with intersegment 'jmp' instruction.
12. The second 16K block of the third 64K segment of system memory is written with zero (0).
13. Both cache sets are enabled.
14. A 'jmp' is made to the start of this 16K block and executed.

15. The ebx register is checked for the correct value.

32. Power-up Test Status. Table 3-6 describes the power-up test status monitored at the CIO port B. (xx means don't care.)

Table 3-6. CPU Power-Up Test Status

Test No.	CIO Port B 7 6 5 4 3 2 1 0	Description
1	0 0 0 0 0 0 0 0	80386 self test
2	0 0 0 0 0 0 1 0	PROM checksum
3	0 0 0 0 0 1 0 0	Cache set 0 data ripple
4	0 0 0 0 0 1 1 0	Cache set 1 data ripple
5	0 0 0 0 1 0 0 0	Cache set 0 address ripple
6	0 0 0 0 1 0 1 0	Cache set 1 address ripple
7	0 0 0 0 1 1 0 0	Cache set 0 content march
8	0 0 0 0 1 1 1 0	Cache set 1 content march
9	0 0 0 1 0 0 0 0	Bus size RAM data ripple
10	0 0 0 1 0 0 1 0	Bus size RAM address ripple
11	0 0 0 1 0 1 0 0	Bus size RAM content
12	0 0 0 1 0 1 1 0	Z8536 CIO
13	0 0 0 1 1 0 0 0	MC146818(RTC) data ripple
14	0 0 0 1 1 0 1 0	MC146818(RTC) address ripple
15	0 0 0 1 1 1 0 0	MC146818(RTC) content/counter
16	0 0 0 1 1 1 1 0	80387/80287 numerical processor
17	0 0 1 0 1 0 0 0	Cacheable page RAM data ripple
18	0 0 1 0 1 0 1 0	Cacheable page RAM address ripple
19	0 0 1 0 1 1 0 0	Cacheable page RAM content
20	0 0 1 1 0 0 0 0	Tag RAM data ripple
21	0 0 1 1 0 0 1 0	Tag RAM address ripple
22	0 0 1 1 0 1 0 0	Tag RAM content
23	0 0 1 1 1 0 0 0	8259A(Interrupt controller)
24	0 1 1 1 1 x x 0	INT5* and INT6*
25	1 0 x x 1 0 0 0	Cache write miss
26	1 0 x x 1 0 1 0	Cache read miss
27	1 0 x x 1 1 0 0	Cache write hit
28	1 0 x x 1 1 1 0	Cache read hit
29	1 0 x x 0 0 0 0	Force cache read miss
30	1 1 x x 1 0 0 0	Tag invalidation
31	1 0 x x 1 0 0 1	Cache execution

Once the preceding tests have been performed, the CPU waits until the primary communications (COMM 0) board is ready to get the results.

If the communications power-up tests pass, the first test summary messages to appear on the system console should be:

```
Communications System Powerup Tests Passed
Initializing system memory
. . . . . .
```

Each dot on the bottom line of the displayed message equals 256K bytes of system memory. For a system with 1M byte of memory, the next test summary messages similar to the following should appear after about 35 seconds:

```
Communications System Powerup Tests Passed
System memory size = xxxxx.
CPU A internal test passed.
CPU A external test passed.
Initializing file processor... ver. x.x passed.
Communications #1 passed.*

Type any key to interrupt autoboot.
```

* If there is a second CPU board installed, you will see more than one CPU message as follows:

```
CPU B internal test passed.
CPU B external test passed.
```

NOTE

If your system has more than two communications boards, you will see more than one communications message, such as **Communications #2 passed,** etc.

If the previous power-up tests failed, refer to Table 3-7 for the power-up error messages with references to the field-replaceable unit (FRU) that may have caused the error message.

Table 3-7. Power-Up Trouble Analysis

Probable Cause	Corrective Action
1. `COMMUNICATION TEST FAILED`	
a. Open or shorted connection to primary communications board	Check primary communications board (COMM 0) and back-plane connectors
b. Fatal error on primary communications board	Replace primary communications board (COMM 0)
2. `COMMUNICATION TEST FAILED: SCC1`	
a. SIO controller IC internal registers are not written and verified	Replace primary communications board (COMM 0)

Table 3-7. Power-Up Trouble Analysis (Cont.)

Probable Cause	Corrective Action

3. `COMMUNICATIONS POWERUP TESTS PASS`
`INITIALIZING SYSTEM MEMORY`
`(No dots appear here)`	

a. Failure in bus clock circuit on CPU board	Replace CPU board
b. Failure on first memory board	Replace first memory board
c. Failure on primary communications board	Replace primary communications board (COMM 0)

4. `COMMUNICATION POWERUP TESTS PASS`
`INITIALIZING SYSTEM MEMORY`
`SYSTEM MEMORY SIZE=4096KB`
`NO RESPONSE FROM CPU A`	

a. Failure on CPU board	Replace CPU board
b. Failure on primary communications board	Replace primary communications board (COMM 0)

5. `COMMUNICATION POWERUP TESTS PASS`
`INITIALIZING SYSTEM MEMORY`
`SYSTEM MEMORY FAILURE`
`CPU A INTERNAL TESTS PASS`
`NO RESPONSE FROM CPU A`	

a. Failure on first memory	Replace the first memory board
b. Failure on CPU board	Replace CPU board

Table 3-7. Power-Up Trouble Analysis (Cont.)

Probable Cause	Corrective Action

6. `COMMUNICATION POWERUP TESTS PASS`
`INITIALIZING SYSTEM MEMORY`
`SIO: SYSTEM BUS ERROR`
`CPU A INTERNAL TESTS PASS`
`NO RESPONSE FROM CPU A`	

a. Failure on first memory board	Replace first memory board
b. Failure on primary communications board	Replace the primary communications board (COMM 0)
c. Failure on CPU board	Replace CPU board

7. `COMMUNICATION SYSTEM POWERUP PASS`
`.....`
`SYSTEM MEMORY FAILURE`
`SIO: SYSTEM BUS ERROR`
`CPU A INTERNAL TESTS PASS`
`NO RESPONSE FROM CPU A`	

a. Failure within first 256K byte block on memory board	Replace correct memory board (check memory configuration)
b. Failure of primary communications board to properly determine system memory size	Replace primary communications board (COMM 0)
c. Failure on CPU	Replace CPU board

Table 3-7. Power-Up Trouble Analysis (Cont.)

Probable Cause	Corrective Action
8.	

```
COMMUNICATION POWERUP TESTS PASS
INITIALIZING SYSTEM MEMORY
SYSTEM MEMORY SIZE = 4096KB
CPU A INTERNAL TEST PASS
CPU A EXTERNAL TEST PASS
NO RESPONSE FROM FILE PROCESSOR

1. BOOT FROM HARD DISK
2. BOOT FROM FLOPPY DISK
3. ENTER MAIN CPU MONITOR
4. ENTER SIO MONITOR
```

a.	Failure of file processor to respond to channel attention from primary communication (COMM 0) board	Replace file processor board
9.		

```
COMMUNICATION POWERUP TESTS PASS
INITIALIZING SYSTEM MEMORY
SYSTEM MEMORY SIZE = 2048KB
CPU A INTERNAL TESTS PASS
CPU A EXTERNAL TESTS PASS
FILE PROCESSOR TEST.....FAILED
XXXXXX WINCHESTER CONTROLLER

1. BOOT FROM HARD DISK
2. BOOT FROM FLOPPY DISK
3. ENTER MAIN CPU MONITOR
4. ENTER SIO MONITOR
```

a.	Failure of device controller IC on controller board	Replace controller board
b.	Failure on file processor board	Replace file processor board

Refer to Table 3-8 for the power-up test failure status monitored at the output latch port B at location 25A on the CPU board.

Table 3-8. CPU Failure Status at Output Latch Port

Test No.	Pin Numbers / Bit Positions 2 / 7	5 / 6	6 / 5	9 / 4	12 / 3	15 / 2	16 / 1	19 / 0	Failed Test
1	0	0	0	0	0	1	1	0	PROM checksum test
2	0	0	0	0	1	0	0	0	Cache data ripple
3	0	0	0	0	1	0	1	0	Cache address ripple
4	0	0	0	0	1	1	0	0	Cache content
5	0	0	0	0	1	1	1	0	Translation data ripple
6	0	0	0	1	0	0	0	0	Translation address ripple
7	0	0	0	1	0	0	1	0	Translation content
8	0	0	0	1	0	1	0	0	Tag data ripple
9	0	0	0	1	0	1	1	0	Tag address ripple
10	0	0	0	1	1	0	0	0	Tag content
11	X	X	X	X	X	X	X	X	Not performed (illegal)
12	X	X	X	X	X	X	X	X	Not performed (illegal)
13	X	X	X	X	X	X	X	X	Not performed (illegal)
14	X	X	X	X	X	X	X	X	Not performed (illegal)
15	0	0	1	0	0	0	1	0	80287 NPX test
16	1	0	0	0	0	0	0	0	Interrupt controller test
17	1	0	1	0	1	0	0	0	Write cache miss
18	1	0	1	0	1	0	1	1	Read cache miss
19	1	0	1	0	1	1	0	0	Write cache hit
20	1	0	1	0	1	1	1	0	Read cache hit
21	1	0	1	1	0	0	0	0	Cache execution test
22	1	1	1	1	0	0	0	1	Tag update
23	1	0	1	1	0	1	0	1	Alternate I/O and memory

File Processor and Controller Power-Up Tests

The file processor and controller firmware consists of power-up diagnostic tests that verify the operation of major components on the file processor and controller boards.

The firmware performs the following tests upon power up. Tests 1 through 12 are done internally within the file processor board while tests 13 and 14 are performed after the file processor gets the first channel attention signal. For tests 1 through 4, the firmware loops on each failed test, and will not proceed to the next test.

For the rest of the tests, the firmware will not loop on each failed test. The firmware attempts to report the power-up status via the printer port (0602h).

The upper four bits of the printer port are used for indicating the test number of the first failed test, while the lower four bits are for displaying the test number of the the last test.

1. **PROM Checksum.** The firmware is located on two 8K x 8 bit PROMS. The checksum byte is written to the last byte of each PROM. Each PROM is checked separately. The sum should be 0 by adding up all the bytes of each PROM.

2. **Local RAM Data Bus Ripple.** This test checks the integrity of the local RAM data bus. A 0 bit pattern is written to location 0000. It then ripples a 1 bit across the data bus to ensure adjacent bits are not stuck.

3. **Local RAM Address Bus Ripple.** This test checks the integrity of the local RAM address bus. A data pattern of decimal 14 is written to local memory location 4000h. Then the data pattern is decremented by 1 and written to the next location by rippling a 1 bit across the address line.

The last location written is 0000h. Each written byte is checked by reading out the written data pattern, writing the complement of that data pattern, and reading back again to verify.

4. **Local RAM Content March.** Each memory word is first filled with a data pattern of 5555h. Each of the 16K words is checked for the data pattern and the complement AAAAh is written back to the same word and verified.

5. **Local Memory Parity Error.** This test checks the local memory parity. For each location tested, an even data pattern (already written during the content march) is read, then the odd data pattern (7676h) is written and dummy read back to verify that a parity error has been generated.

6. 8254. This test programs counter 0 of interval timer 8254 for mode 0, loads counter 0, and starts the count. After a short delay, the counter is read back to verify that the counter has been decremented.

7. DMA Controller. This test programs interval timer 8254 to generate an interrupt signal to the IRO pin of the interrupt controller 8259. The interrupt controller is then verified.

8. SCSI Controller. Upon power-up or reset, the controller will perform self-diagnostics. When self-diagnostics are complete and if no error was detected, the diagnostic-status register is checked for bit pattern 10000000 which verifies the SCSI controller.

9. DMA Controller. This test first clears each channel-status register by writing FFh into the register. Then a 5678h pattern is written to the memory-transfer counter for each DMA channel and each memory-transfer counter is verified later.

10. Floppy Disk Controller. To verify the floppy-disk interface, the firmware first issues a SPECIFY command to set the initial values for each of the three internal timers (head unload time, step rate time, and head load time). Then it issues a RECAL command to initialize the drive and retract the heads. If no error is detected, the interface is verified.

11. Hard Disk Controller. This test first writes six different data patterns to six internal registers of DP8466. Each of the six registers is checked for the corresponding data pattern and the complement of that data pattern is written to the same register and verified.

12. Streaming Tape Controller. The interface is verified by checking that reset/power (bit 0) is set in status byte 1. Then the Self Test 1 command is performed to verify the controller.

13. System RAM Data-Bus Ripple. This test checks the system RAM data bus. A 0 pattern is written to system-memory word 00000. Then a 1 bit is rippled across the data bus to ensure that adjacent bits are not stuck.

14. System RAM Address-Bus Ripple. This test checks the system RAM address bus. A data pattern of decimal 19 is written to local memory location 80000h. Then the data pattern is decremented by 1

and written to the next location by rippling a 1 bit across the address line. The last location written is 00000h.

Then each byte is checked by reading the data pattern, writing the complement of that data pattern, and reading back again to verify.

CPU AND FILE PROCESSOR COMMUNICATION

Software interface between the CPU board and file processor board is by means of a parameter block. At initialization, location 1FFFCh to 1FFFFh in system memory contains a pointer to this parameter block. The first time the file processor is interrupted, the pointer is read to locate the parameter block.

Interrupt Signals

The basic communications interface between the CPU board and file processor board is via two signals:

1. **386INT (channel attention to file processor).** When this signal is asserted by performing an I/O write to system I/O address 000Eh, the file processor is informed that a control block created by the CPU board is available or the previous command request from the file processor has been executed.

2. **INT386 (channel attention to CPU board).** When this signal is asserted, the CPU board is informed that a control block created by the file processor is available or the previous command request from the CPU board has been executed.

Communication Protocol

Upon completion of all internal tests, the file processor waits for the first channel attention from the primary communications board. As soon as channel attention occurs, the file processor gets the control block pointer in system memory location 1FFFC and obtains all the information from the control block.

The device number (word) and the command (word) should be 12 (file processor) and 0 (power-up initialization) respectively.

The file processor writes a hexadecimal value of FF to the result (word) indicating that the command has been accepted. Then the file processor performs a system data-bus and system address-bus ripple test.

Upon completion, the file processor puts the power-up test result message in the message buffer, stores the status in the result word, and clears the command pending bit (bit 15 of the command word). The file processor then remains in an idle state and waits for the subsequent CPU channel attention.

When the next CPU channel attention occurs, the file processor obtains the command information from the control block, writes a hexadecimal value of FF to the result word for acknowledging, branches to the appropriate routine for executing the command, puts the status in the result word, clears the command pending bit, and sends an interrupt to the CPU board. Then the file processor goes back to the idle state and waits for a channel attention from the CPU board.

Boot Failures

If all power-up tests have passed, the message **Type any character to interrupt autoboot** appears. Press any key within the next five seconds. The screen then displays a boot menu similar to:

```
Enter <1> to Boot from Hard Disk
Enter <2> to Boot from Floppy Disk
Enter <3> to enter the main CPU Monitor
Enter <4> to enter the main (Multidrop or SIO) Monitor
```

If you did not press a key within five seconds, the system will attempt a default boot (autoboot) from the hard disk. This is normal start-up procedure after you install the operating system software.

If the autoboot failed or if you entered a **1**, and the boot from the hard disk failed, a message similar to the following will appear:

```
Booting from hard disk
File system not supported
Boot failed, status: 00 00 00 00 00

Select <1> to boot from Hard Disk
Select <2> to boot from Floppy Disk
Select <3> to enter Debugger
```

Status bytes 1 through 5 in the preceding **Boot failed, status: 00 00 00 00 00** message indicates the hard disk status as follows:

RESULTS BYTE 1:

0 = No error
1 = General error
2 = Device not supported
3 = Device not present
4 = Invalid command
5 = Interrupt/DMA operations error
6 = National Semiconductor DP8466 hard disk controller command error
FF = Command accepted, but not yet finished

RESULTS BYTE 2: Contains the low byte of the ESDI drive's standard status.

RESULTS BYTE 3: Contains the high byte of the ESDI drive's standard status.

RESULTS BYTE 4: Contains the contents of the DP8466 status register. Refer to Table 3-10 for a detailed description of the status register bits.

RESULTS BYTE 5: Contains the contents of the DP8466 error register. Refer to Table 3-9 for a detailed description of the error register bits. Refer to the *National Semiconductor Data Book* for additional information.

Table 3-9. Hard-Disk Controller Error Register Bit Descriptions

Bit No.	Bit Name	Symbol	Description
7	Late Interlock	LI	Occurs only if IR bit in OC register is set. Set if controlling logic has failed to write to the interlock (HBC) register before the end of the data field of the present sector
6	Correction Failed	CF	Set if correction is attempted (SCC bit set in OC register) and correction failed
5	FIFO Data Lost	FDL	Set during a disk read operation if the FIFO overflows, or during a disk write operation if the FIFO is read when it is empty
4	No Data Synch	NDS	Set if a sector or index pusle occurs while the DDC is waiting to byte align on the first data synch field (synch #1 or #2), or if the DCC byte aligns to the first synch word of the data field but does not match to subsequent bytes (synch #1 or #2)
3	Sector Overrun	SO	Set if RGATE is active and FIFO is being written to when a sector or index pulse is received. If WGATE is active, this bit is set when a sector or index pulse is received
2	Sector Not Found	SNF	Set when header cannot be matched for two consecutive index pulses in any compare- header operation

Table 3-9. Hard-Disk Controller Error Register Bit Descriptions (Cont.)

Bit No.	Bit Name	Symbol	Description
1	Data Field Error	DFE	Set when a data field CRC/ECC error is detected in a read-data or check-data operation. May be set when another error occurs; especially an error that occurs during a write operation. These errors would be Sector Overrun or FIFO Data Lost
0	Header Failed Although Sector Number Matched	HFASM	Set when the header byte(s) marked with the EHF bit in the corresponding HC register(s) matched correctly, but other header bytes were in error

Table 3-10. Hard-Disk Controller Status Register Bit Descriptions

Bit No.	Bit Name	Symbol	Description
7	Error Detected	ED	Set on assertion of one or more bits in the Error register
6	Correction Cycle	CCA	Set on assertion of SCC bit in the OC register
5	Local Command	LCB	Set when command requiring local DMA is loaded
4	Remote Command Busy	RCB	Non-Tracking Mode: Set when OC register is loaded with a DMA instruction Tracking Mode: Set when RRQ pin is first asserted in a disk-write mode, or when the Drive Command register is loaded in a disk-read mode
3	Local Request	LRQ	Set when LRQ pin is assserted
2	Header Match Completed	HMC	Compare Header Operation: Set when header field is correctly matched with no CRC/ECC error Read Header Operation: Set when header field has been read with no CRC/ECC error
1	Next Disk Command	NDC	Set to allow the DDC to accept a new command into the DC register
0	Header Fault	HF	Set when an CRC/ECC error is detected in a header field

If you entered a 2 and the boot from floppy disk failed, a message similar to the following will appear:

```
Booting from floppy (low speed)
Boot failed, status: 00 00 00 00 00

Select <1> to boot from Hard Disk
Select <2> to boot from Floppy Disk
Select <3> to enter Debugger
```

Status bytes 1 through 5 in the preceding **Boot failed, status: XX XX XX XX XX** message indicate the following floppy disk status:

RESULTS BYTE 1:

0 = No error
1 = General error
2 = Device not supported
3 = Device not present
4 = Invalid command
5 = Interrupt/DMA operations error
6 = NEC PD765 floppy disk controller command/status error
FF = Command accepted, but not yet finished

RESULTS BYTE 2: Contains the contents of the PD765 status register 0. Refer to Table 3-11 for a detailed description of the status register 0 bits.

RESULTS BYTE 3: Contains the contents of the PD765 status register 1. Refer to Table 3-12 for a detailed description of the status register 1 bits.

RESULTS BYTE 4: Contains the contents of the PD765 status register 2. Refer to Table 3-13 for a detailed description of the status register 2 bits.

RESULTS BYTE 5: Contains the contents of the PD765 status register 3 (not generally reported). Refer to Table 3-14 for a detailed description of the status register 3 bits.

Refer to the *NEC PD765 Data Book* for additional information.

Table 3-11. Floppy Disk Controller Status Register 0 Bit Descriptions

Bit No.	Bit Name	Symbol	Description
7	Inter-rupt Cod	IC	D7 and D6 = 0. Normal termination of command (NT). Command complete and properly executed
6	------		D7 = 0 and D6 = 1. Abnormal termination of command (AT). Execution of command started but not successfully completed D7 = 1 and D6 = 0. Invalid command issued. Command was issued but not started D7 and D6 = 1. Abnormal termination caused by the Ready line from FDD changing states during command execution
5	Seek End	SE	When the PD765 controller (FDC) has completed a seek, the Seek command line = 1
4	Equipment Check	EC	Asserted if the fault signal is received from the floppy disk drive (FDD) or if the track 0 signal fails to occur after 77 step pulses (recalibrate)
3	Not Ready	NR	Asserted when FDD is in the not ready state and a read or write bit is set. Command occurs if a read or write is issued to side 1 of a single-sided drive, then flag is set

Table 3-11. Floppy Disk Controller Status Register 0 Bit Descriptions (Cont.)

Bit No.	Bit Name	Symbol	Description
2	Head Address	HD	Flag used to indicate the state of the head at interrupt
1	Unit Select 1	US1	Flag used to indicate a drive unit interrupt
0	Unit Select 0	US0	Flag used to indicate a drive unit at interrupt

Table 3-12. Floppy Disk Controller Status Register 1 Bit Descriptions

Bit No.	Bit Name	Symbol	Description
D7	End of Cylinder	EN	Set when PD765 controller (FDC) to access a sector beyond the final sector of a cylinder
D6	-------		Not used. Always zero (0)
D5	Data Error	DE	Set when FDC detects a CRC error in either the (ID) or data fields
D4	Overrun	OR	Set if the FDC is not serviced within a certain time during data transfers by the main system
D3	-------		Not used. Always zero (0)

Table 3-12. Floppy Disk Controller Status Register 1 Bit Descriptions (Cont.)

Bit No.	Bit Name	Symbol	Description
D2	No Data	ND	Set if, during execution of the Read Data, Write, Deleted, or Scan commands, the FDC cannot find the sector specified in the IDR register Set if, during execution of the Read ID command, the FDC cannot read the ID field without an error Set if, during execution of the Read or Cylinder commands, the starting sector cannot be found
D1	Not Writable	NW	Set if, during execution of Write Data, Write Deleted Data, or Format a Cylinder, the FDC detects write protect signal from FDD
0	Missing	MA	Set if the FDC cannot detect the address mark or deleted data address mark. Also altos mark. Also, at the same time, MD (missing address mark in data field) in status register is set. Also set if FDC cannot detect ID address mark during two index pulses

Table 3-13. Floppy Disk Controller Status Register 2 Bit Descriptions

Bit No.	Bit Name	Symbol	Description
7	------		Not used. Always zero (0)
6	Control Mark	CM	Set if, during execution of the Read Data or Scan commands, the PD765 controller (FDC) encounters a sector that contains a deleted data address mark
5	Data Error Data Field	DD	Set if the FDC detects a CRC error in the data field
4	Wrong Cylinder	WC	Related to ND. Set when the content of C on the medium is different from that stored in IDR
3	Scan Equal Hit	SH	Set if, during execution of the SCAN command, the condition of "equal" is satisfied
2	Scan Not Satisfied	SN	Set if, during execution of the Scan command, the FDC cannot find a Sector on the cylinder that meets the condition of "equal" in the above command
1	Bad Cylinder	BC	Related to ND. Set when the content of C on the medium is different from that stored in the IDR and the content of C is FF
0	Missing Address Mark in Data Field	MD	Set if, when data is read from the medium, the FDC cannot find a Data Address Mark or Deleted Data Address Mark

Table 3-14. Floppy Disk Controller Status Register 3 Bit Descriptions

Bit No.	Bit Name	Symbol	Description
			NOTE The following data is available in the parameter block and is not written to the screen
D7	Fault	FT	Indicates the status of the Fault signal from FDD
D6	Write Protect	WP	Indicates the status of the Write Protect signal from FDD
D5	Ready	RY	Indicates the status of the Ready signal from FDD
D4	Track 0	T0	Indicates the status of the Track 0 signal from FDD
D3	Two Side	TS	Indicates the status of the Two Side signal from FDD
D2	Head Address	HD	Indicates the status of the Side Select signal to FDD
D1	Unit Select 1	US1	Indicates the status of the Unit Select 1 signal to the FDD
D0	Unit Select 0	US0	Indicates the status of the Unit 0 signal to the FDD

Entering a 3 from the boot menu (or from the menu that appears when the boot fails) gets you into the CPU monitor debugger and a message from the CPU board similar to the following appears:

```
CPU A Monitor/Debugger          V1.X
Type ? For Help Menu
CS:IP = 0018:26B2
```

Entering a **4** from the boot menu gets you the primary communications monitor debugger and a message from the communications board similar to the following will appear:

```
Multidrop Communications Monitor/Debugger-Version X.X
Type ? for the Menu
MDC Memory Size = 512KB
```

If a **failed** message appears in the power-up test summary, determine which tests in the SDX Field Service Menu are applicable and run the tests. If desired, use the boot menu to select the CPU or primary communications debuggers (monitors) and perform the debugger procedures as described in **Monitor Debugger** - Chapter 5.

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Chapter 4
Floppy-Based Diagnostics

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SYSTEM-CONFIDENCE TESTS

The system-confidence tests use diagnostic programs contained on the System Diagnostic Executive (SDX) floppy disk included with the Series 2000. The system-confidence tests are designed for the operator or less experienced technician to perform a series of menu-driven tests that are more thorough than the previous power-up tests. The system-confidence tests contain a set of system utilities for handling system configuration and storage devices.

The system-confidence tests dynamically test the following:

- floppy disk drive
- hard disk drive
- controller
- serial communication channels
- central processing unit (CPU)
- system memory
- file processor
- interrupt controller

System-confidence tests should be run if you are not sure there is a problem (i.e., sporadic failures), or to help determine if a problem is hardware or software related. The non-destructive system-confidence tests take about 15 to 30 minutes and verify most of the hardware, but only give a pass/fail indication.

Booting the SDX Disk

Perform the following procedure to boot the SDX floppy into memory to enable you to run the system-confidence tests:

NOTE

The SDX diagnostics will not boot from the disk if the computer is connected to any multidrop or WorkNet network. If there are any devices networked to the computer, notify the users to save their data before disconnecting the computer from the network.

1. Insert the SDX disk into the floppy drive and obtain the boot menu as described in **Power-Up Checks** - Chapter 3.

2. Type **2** to boot from the SDX floppy disk. Wait for the SDX menu to appear as follows:

```
ACS xxxx SYSTEM DIAGNOSTIC EXECUTIVE (SDX)
                        Version vx.x

Main Menu:

   R:  Run system confidence tests

   U:  Utility programs

   S:  Display test summary

   X:  Exit System Diagnostic Executive (SDX)


 *** Enter command and press <Retn>:
```

3. Type **r** and press Retn to begin the system confidence tests. If you want to stop the test process, press Esc several times. The testing will stop with the current test (sometimes it takes a while).

   The Main Memory Refresh Test takes two minutes. Although it is not recommended that any test be bypassed, you can bypass this test by pressing Esc immediately after the message:

```
Memory Refresh Test in progress, press <Esc> to abort this test.
```

NOTE

You do not need to monitor this test. The program saves the test results which you can review after the tests are completed.

4. Take a break while the tests complete. The test summary is ready when you see the following message:

```
Do you wish to review test summary (y or n):
```

After you type **y**, the screen displays information similar to:

```
System Confidence Tests Summary

PROM Checksum Test                      Passed
Cache RAM Test                          Passed
Translation RAM Test                    Passed
Memory Management Unit Test             Passed
Numerical Processor Test                Not Present
Main Memory March Test                  Passed
Main Memory Refresh Test                Passed
Floppy Random Seek Test                 Passed
Hard Disk Verify Test                   Passed
Streaming Tape Append Test              Passed
SIO PROM Checksum Test                  Not Present
SIO Memory March and Refresh Test       Not Present
SIO LSI Chips Access Test               Not Present
SIO Interrupt Vector Test               Not Present
SIO DMA Test                            Not Present
SIO Timer Test                          Not Present
MDC PROM Checksum Test                  Passed
MDC System Bus Addressability Test      Passed
MDC Memory March and Refresh Test       Passed
MDC LSI Chips Access Test               Passed
MDC Interrupt Test                      Passed
MDC DMA Test                            Passed
MDC Timer Test                          Passed
MDC Baud Rate Test                      Passed
```

If you need to stop the system-confidence tests before they are completed, press **Del**. The message **Interrupted** appears and you will return to the Main Menu. If you want to stop the current test and continue to the next test, press **Esc**. You can also review the test summary by selecting **s** from the Main Menu.

If the test summary reports any tests as **Failed**, note the test description in the test summary and replace the failed field-replaceable unit (FRU) or perform the appropriate tests in the Field Diagnostic Executive Menu as described under "Field-Service Tests."

FIELD-SERVICE TESTS

The field-service diagnostic tests (FDX) are contained on a floppy disk included as part of the maintenance package available from Altos Customer Support. These tests are the most thorough and flexible tests available to service personnel. The system can be tested extensively by running the field-service tests individually and repeatedly.

Unlike the system-confidence diagnostic tests (SDX), the field-service diagnostic tests include commands for looping tests, changing parameters, and selecting debugger routines (refer to **Monitor Debugger - Chapter 5** for a description of the debugger routines). The field-service tests are potentially destructive and can erase the contents of the hard disk.

The field-service tests can be individually selected and report pass/fail messages to the terminal. Five different test menus are accessed through the Field Diagnostic Executive Menu to provide options for testing the CPU, file processor and controller, and communications (SIO and multidrop) circuits. Detailed error messages are saved in a history buffer that allows you to recall them from the Field Diagnostic Executive Menu at any time.

NOTE

The field-service tests described in this chapter are for version V1.0 of the FDX diagnostics.

Field Diagnostic Executive Menu

Perform the following procedure to boot the FDX disk and obtain the Field Diagnostic Executive Menu:

NOTE

The FDX diagnostics will not boot from the disk if the computer is connected to any multidrop or WorkNet network. If there are any devices networked to the computer, notify the users to save their data before disconnecting the computer from the network.

1. Boot the FDX floppy disk as described under "Booting the FDX Disk" in **Utilities** - Appendix B. The following FDX Field Diagnostic Executive Menu will appear:

```
Field Diagnostic Executive Menu:

b (brief)       Brief description of all tests
c (clear)       Clear pass count, error count, and history
d (disable)     Disable test
e (enable)      Enable test
h (halt)        Halt on error
l (loop)        Loop on command line
m (menu)        Menu level selection
p (parameter)   Change parameters
r (report)      Display error history
s (summary)     Display error summary
t (test)        Execute test(s)
u (utility)     Call utility programs
(help)        Display this menu
x (exit)        Exit to main menu
z (debugger)    Enter debugger

***Enter Command and Press <Retn>:
```

2. Type the appropriate command from the Field Diagnostic Executive Menu to perform the following test functions:

   b (brief). Displays a brief description of all the FDX tests with their test number and enabled or disabled status.

   c (clear). Clears the error history buffer and resets the pass count and error count to zero.

   d (disable). Allows you to disable any selected tests executed by the **t** command as follows:

   a. Enter the test number(s), separated by commas, or press Retn for all tests, or Esc to exit the tests.

   b. Press Retn.

   e (enable). Allows you to enable tests to be executed by the **t** command as follows:

   a. Enter the test number(s), separated by commas, or press Retn for all tests, or Esc to exit the tests.

   b. Press Retn.

   h (halt). Allows you to choose from two options for running the **t** tests: (a) the tests halt when an error occurs and (b) the program continues after an error is discovered or until the end of the test.

   l (loop). Allows you to select the number of times a test will run. Press Del to abort or Retn to loop indefinitely.

   m (menu). Allows you to select from four menu options which are displayed during the execution of the **t** tests: (a) displays all the menus, (b) stops the help menu from appearing after each command is entered, (c) stops the test menus from being displayed after the **t** command has been typed, and (d) allows the test or help menus to be displayed if a **?** or **b** is typed.

p (parameter). Allows you to change the SIO/MDC parameters from their default settings as follows:

a. The following Parameter Menu appears after the **p** and Retn are typed.

```
Parameter Menu:

Parameter #   Parameter Description

1             SIO/MDC Parameters
2             Return to previous menu

Enter Selection:
```

b. Press **1** to obtain the following SIO/MDC Port Configuration display:

```
                    PORT CONFIGURATION

Hardware      Software      Baud  Stop  Parity  Test
Name          Name          Rate  Bit   Bit     Status
-------------------------------------------------------
MDC 0, Port 0 tty0/Console  9600  1     OFF     Disabled
MDC 0, Port 1 tty1          9600  1     OFF     Enabled
MDC 0, Port 2 tty2          9600  1     OFF     Enabled
MDC 0, Port 3 tty3          9600  1     OFF     Enabled
MDC 0, Port 4 tty4/WorkNet  9600  1     OFF     Enabled
SIO 1, Port 0 tty5          9600  1     OFF     Enabled
SIO 1, Port 1 tty6          9600  1     OFF     Enabled
SIO 1, Port 2 tty7          9600  1     OFF     Enabled
SIO 1, Port 3 tty8          9600  1     OFF     Enabled
SIO 1, Port 4 tty9          9600  1     OFF     Enabled

command:  (c)hange, (d)isplay, (h)elp (q)uit without change,
          (s)ave the changes and exit

Type a command (c, d, h, q, or s) and press <Retn>
Enter:
```

c. Answer the prompts in the order presented and follow each entry with a Retn. When the last prompt is answered, the SIO/MDC Parameters display will then appear so that you can recheck your SIO/MDC parameter changes.

r (report). Displays the error history of specified tests.

s (summary). Displays the name and number of all tests run, the number of passes run, and the number of errors detected.

t (test). Begins running any tests in the order specified.

u (utility). Displays the utility menu.

? (help). Displays the Field Diagnostics Executive Menu.

x (exit). Returns to the Main Menu.

z (debugger). Enters the debugger.

CPU Test Menu

Perform the following procedure to obtain the CPU Test Menu:

1. Press **t** while in the Field Diagnostic Executive Menu. The first menu displayed is the CPU Test Menu:

```
CPU Test Menu:

Test #     Description                                  Status

1      CPU PROM Checksum Test                           Enabled
2      CPU MMU/ALU Test                                 Enabled
3      CPU Cache RAM Test                               Enabled
4      CPU Bus Size RAM Test                            Enabled
5      CPU Cacheable Page RAM Test                      Enabled
6      CPU Tag RAM Test                                 Enabled
7      CPU CIO Test                                     Enabled
8      CPU PIC Interrupt Test                           Enabled
9      CPU Real Time Clock                              Enabled
10     CPU Cache Functional Test                        Enabled
11     CPU 80387 Numeric Processor Extension Test       Enabled
12     Memory Tests                                     Enabled
N      Display Next Test Menu
R      Return to Field Service Menu


Enter test numbers, separated by commas, followed by <Retn>
Press <Retn> to execute all tests
Press <Esc> for next test or <Del> to exit testing

Enter:
```

2. Type the appropriate command from the CPU Test Menu to perform the following test functions:

1 PROM Checksum Test. The PROMs are summed separately to indicate which one is bad. A failure of the checksum is considered a major failure because the integrity of the PROMs is in doubt.

2 CPU MMU/ALU Test. The CPU MMU/ALU test consists of three subtests as follows:

MMU Operation. This test verifies that the memory management unit of the 80386 microprocessor is functional. This is done by operating a mini-multitasking scheduler with three independent tasks. A total of 40 task switches are done. There is one controlling task and two subtasks. After the scheduler is done, a check is made to find out if it operated correctly. Note each task has its own TSS, LDT, code segment, data segment, and also the necessary system descriptors.

CPU Paging. This test consists of two parts: the first part verifies the paging mechanism of the 80386 CPU and the second part verifies the generation mechanism of exception 14.

The first part installs the page directory and page table in system memory with 1:1 mapping. The test reads data from 240 different pages into a relocatable buffer with paging disabled. Then the same read sequence is performed with a different buffer but with paging enabled. Because of the 1:1 mapping the two buffers should be the same if the paging mechanism is functioning properly. If the buffers differ, then the first part of the paging test has failed.

The second part of the paging test verifies that the page fault (exception 14) mechanism is functioning. To create a page fault exception, the page is intentionally made "non-present" and data is accessed from that page. This sequence transfers control to the exception handler, where the page is made "present" and the interrupted instruction is restarted. If the following steps were not executed, the data accessed from that page will be invalid and this test fails.

Exception-Handling Facility. This test ensures that the exception-handling facility and arithmetic operations of the arithmetic logic unit are functional.

This test intentionally causes an exception 13 and 11 to verify the operation of the 80386 CPU protection mechanism. To create an exception 13, the memory access is made outside of the segment, thus exceeding the segment's limit. This action transfers control to the exception 13 handler, where the limit is increased to allow the memory access to be restarted. The exception handler can separate between an intentional and a real exception 13 by testing a global flag (initialized by the test routine) to a value of 55AAAA55h.

If the exception 13 was created on purpose, the exception handler inverts this flag to let the test routine know that an exception 13 has occurred. In addition, the message "Valid Exception 13 has been generated" is printed. The test checks that the value of the global flag is AA5555AAh; if so, the test passed, if not the test failed.

The exception 11 generation is tested similar to the exception 14 and 13 tests. A "non-present" segment descriptor is created and this discriptor is used to try to access data in memory. The descriptor is made "present" again in the exception handler and, similar to the exception 13 test, a global flag is inverted to let the test routine know that execution control was transfered to the exception 11 handler. The exception 11 handler prints the message "Valid Exception 11 has been generated" if the exception 11 has occurred on purpose. The test fails if the global flag was not inverted by the exception 11 handler.

3 CPU Cache RAM Test. The cache RAM test consists of six subtests as follows:

Cache RAM Set 0 Data Ripple. The cache RAM set 0 is located from 10000000h to 10003FFFh. The first two double words (8 bytes) are used to test the data lines. A one (1) is rippled through the data lines then a zero (0) is rippled through.

Cache RAM Set 1 Data Ripple. The cache RAM set 1 is located from 10004000h to 10007FFFh. The first two double words (8 bytes) are used to test the data lines. A one (1) is rippled through the data lines then a zero (0) is rippled through.

Cache RAM Set 0 Address Ripple. Eight locations of the cache RAM set 0 are loaded with different background patterns.

Then, each selected location is checked by reading out the written pattern, writing the complement of the data pattern, and reading back again to verify.

Cache RAM Set 1 Address Ripple. Eight locations of the cache RAM set 1 are loaded with different background patterns. Then, each selected location is checked by reading out the written pattern, writing the complement of the data pattern, and reading back again to verify.

Set 0 Content March. The cache RAM set 0 is tested with two patterns; 55h and AAh. This test first writes the whole set of cache with 55h, two words at a time. Then, it reads the data and writes its complement, one byte at a time. This test leaves data pattern AAh in the cache RAM.

Set 1 Content March. The cache RAM set 1 is tested with two patterns; 55h and AAh. This test first writes the whole set of cache with 55h, two words at a time. Then, it reads the data and writes its complement, one byte at a time. This test leaves data pattern AAh in the cache RAM.

4 CPU Bus Size RAM Test. The CPU bus size RAM test consists of three subtests as follows:

Bus Size RAM Data Ripple. The bus size RAM is located from 14000000 to 17FFFFFFh. The first double word (4 bytes) is used to test the data lines. Only two data lines need to be tested. Four different patterns (bit 29,28 = 00,01,10,11) are used in this test.

Bus Size RAM Address Ripple. This test checks the integrity of the bus size RAM address bus. There are 12 address lines to test. A one (1) is rippled through the address lines then a zero (0) is rippled through. First, the whole RAM is writ-

ten with a pattern. Then, each address location is read, checked, and complemented. This procedure is done for both patterns.

Bus Size RAM Content. The bus size RAM is tested with four patterns (bit 29,28 = 00,01,10,11). Each location is tested with all four patterns before moving on to the next location.

5 CPU Cacheable Page RAM Test. The cacheable page RAM test consists of three subtests as follows:

Data Ripple. The cacheable page RAM is located from 08000000 to 0800FFFFh. The first double words (4 bytes) are used to test the data lines. There are two data lines (TD30 and TD31) to test. Four different patterns (bit 31,30 = 00,01,10,11) are used in this test.

Address Ripple. This test checks the integrity of the cacheable page RAM address bus. There are fourteen address lines to test. A one (1) is rippled through the address lines then a zero (0) is rippled through.

RAM Content. The cacheable page RAM is tested with two patterns (bit 31,30 = 01,10). The test first writes the whole RAM with pattern 01. Then, it reads the data and writes its complement. Finally, it writes the whole RAM with pattern 11 to leave all ones (1s) in the cacheable page RAM.

6 CPU Tag RAM Test. The tag RAM test consists of three subtests as follows:

Tag RAM Data Ripple. The tag RAM is located from 0C000000 to 0C003FFFh. There are 28 data lines to test. The first double word location is used to test the data lines. A one (1) is rippled through the data lines then a zero (0) is rippled through.

Tag RAM Address Ripple. This test checks the integrity of the tag RAM address bus. If the cache block size is configured to 4 bytes, there there are 12 address lines to test. If the cache block size is configured to 8 bytes, there are 11 address lines to test. A one (1) is rippled through the address lines then a zero (0) is rippled through.

Tag RAM Content March. The tag RAM is tested with two patterns; 55h and AAh. For a 4-byte cache block size, there are 4K locations to test. Otherwise, (if the cache block size is 8 bytes) there are only 2K locations to test. This test first writes the whole RAM with 55h, two words at a time. Then, it reads the data and writes its complement.

7 CPU CIO Test. This test first reads back the contents of two internal registers which have been initialized upon power up. Then, it tests the counter/timer 1 time constant register (MSB) by rippling a one (1) through the data lines. Finally, all three timers are set up to run independently and the command/ status registers are read to verify that all three counters are exhausted.

8 CPU PIC Interrupt Test. The CPU PIC interrupt test consists of two subtests as follows:

Register. The PIC is set up for fully nested, no buffer, auto EOI, 8086-mode of operation. Then OCW1 is written and read back nine times to test if the chip is functional.

IR0, INT5*, and INT6*.* This test ensures that interrupts can be serviced asynchronously. The INT0 is tested through the CIO timer interrupt. The INT5 and INT6 are tested separately through the CIO port B. If these interrupts are detected, the test passes.

9 CPU Real Time Clock Test. The CPU real time clock test consists of three subtests. Before executing the subtests described below, a prolog procedure is executed for each subtest. This prolog procedure verifies the operation of the nonvolatile RAM.

If there is no battery installed (or if the battery is bad) and the power is turned off and then on again, the three subtests are executed and will yield a failure status. If the test reports a failure, it is necessary to go to the FDX Utility Menu and select the Real Time Clock Utility and reinitialize the non-volatile RAM. See **Reference Information** - Appendix B.

Data Ripple. The real time clock is located from 18000000 to 1800007Fh. There are eight data lines to test. The internal RAM location 0eh is used to test the data lines. A one (1) is rippled through the data lines then a zero (0) is rippled through.

Address Ripple. This test writes to seven selected locations using the address as the background pattern. Then each location is read back to verify.

Content. There are 50 read/write locations in the chips and all of them are tested with two patterns; 55h, AAh, 00h, and FFh, one byte at a time. At the end of the test, the last three bytes of RAM are written with 59h, 52h, and 19h to indicate that the clock chip has been tested and initialized. These three locations are reserved by the monitor. This subtest will also ensure that the real time clock is keeping time properly.

10 CPU Cache Functional Test. The cache functional test consists of seven subtests as follows:

Cache Write Miss. The cache is turned off and the cache RAM is filled with zeros (0s). Then, the tags are made invalid and the cache is turned on. Ones (1s) are written to 32K of system memory at 50000h. The cache is again turned off and checked to see that it is still filled with zeros (0s). This test ensures that there is no caching during a write operation.

Cache Read Miss. Four 16K blocks of memory are written at 50000h and the following test sequence is performed:

1. Cache 0 is enabled and cache 1 is disabled and the first 16K block is read.

2. Cache 0 is disabled and checked to determine that it has been updated.

3. Cache 1 is enabled and the second 16K block is read.

4. Cache 1 is disabled and checked to determine that it has been updated.

5. Both cache sets are enabled and the third 16K block is read.

6. Both cache sets are disabled and cache 0 is checked for proper values. Also, the tags are checked to see that they contain the proper value.

7. Both cache sets are enabled and the forth 16K block is read.

8. Both cache sets are disabled and cache 1 is checked for the proper values. Also, the tags are checked for proper values.

Cache Write Hit. All the tags are made valid. Both cache sets are enabled. Then, 32K of system memory at 50000h are written with zeros (0s). Both cache sets are disabled and verified that the contents of both sets are zero (0).

Cache Read Hit. The tags are made valid and both cache sets are disabled and 32K of system memory at 50000h is set to zero (0). Then, both cache sets are loaded with FFh. Both cache sets are enabled and the system memory is read and checked for the FFh pattern. This test checks that data comes from the cache instead of memory.

Force Cache Read Miss. Tags are made valid. The contents of both cache sets are set to FFh and 32K of system memory is set to zero (0). Both cache sets are enabled. The CMISS* bit is set to 0 and 32K of system memory at 50000h is read and checked for zero (0).

Tag Invalidation. The tags are made valid. Both cache sets are enabled and TSTBIT is set to simulate a write from another bus master. A 32K block of system memory at 50000h is written with FFh. Then, the tags are checked to see if the valid bits are set to invalid.

Cache Execution. The contents of both cache sets are copied to buffer at 40000h before the test and copied back after the test. Since GDT/IDT resides in cache set 0, GDT/IDT is also relocated to non-cacheable RAM before the test and copied back after the test. Note that before running this test all pages below 50000h are declared non-cacheable.

This subtest makes two passes for each cache set. In the first pass a check is made if the data can be "cached" into the cache (10000000-10007FFF).

Initially, the cache is filled with garbage data and then a program (16K byte buffer located at 50000h) is loaded into cacheable page system RAM and executed. Then, the contents of the cache is compared with the program (located at 50000h) residing in cacheable system RAM. In the second pass, a check is made to determine if the cached data from the first pass can be executed from the cache itself. This test also verifies that both "the cache read" and "cache miss" mechanism of the caches operates correctly.

11 CPU 80387 Numeric Processor Extension Test. This test verifies that the 80387 numeric processor extension is functional. If it is not present, the test yields untested status. Many numeric processor primitives are tested including add, subtract, divide, and multiply.

12 Memory Test. The memory test consists of three subtests as follows:

Address. This test disables the NMIs and sizes memory. If there is a hole in memory, the test will fail. This test then writes an incrementing word pattern to each word location in memory and compares for the incrementing pattern in memory. Then, it will write the opposite of the word pattern to each word location. This test will fail for a data miscompare.

March. This test disables the NMIs and sizes memory. If there is a hole in memory, the test will fail. This test writes 5555h to each word location, verifies each word location, enables NMIs, and then writes AAAAh to each word location. Each word location is verified for the correct data and to ensure that an NMI did not occur. This test will fail for a data miscompare or if an NMI occurred.

Refresh. This test enables the NMIs and sizes memory. If there is a hole in memory, the test will fail. This test writes 0000h to each word location and executes out of cache memory for approximately 1 minute, then verifies that memory is 0000h. Then the test writes FFFFh to each word location,

sleeps, and then verifies that memory is all FFFFh. This test will fail if a data miscompare or an NMI occurs.

File Processor and Controller Test Menu

Perform the following procedure to obtain the File Processor and Controller Test Menu:

1. Press **n** and note that the second menu displayed is the File Processor and Controller Test Menu:

```
File Processor and Controller Test Menu

Test # Description                    Status

13      Hard Disk Write/Read Test     Enabled
14      Hard Disk Random Seek Test    Enabled
15      Hard Disk Verify Test         Enabled
16      Systems Test                  Enabled
17      Tape Append Test              Enabled
18      Tape Write/Read Test          Enabled
19      Floppy Random Seek Test       Enabled
20      Floppy Write/Read Test        Enabled
N       Display Next Test Menu
R       Return to Field Service Menu

Enter test numbers, separated by commas, followed by <Retn>
Press <Retn> to execute all tests
Press <Esc> for next test or <Del> to exit testing

Enter:
```

2. Type the appropriate command from the File Processor and Controller Board Test Menu to perform the following tests:

   13 Hard Disk Read/Write Test. This test reads then writes the entire surface of the hard disk. In the first part of this test, you must select the drive that is to be tested.

The Hard Disk Read/Write Test destroys any operating system that has been installed on the hard disk as the following message warns you:

```
This test will destroy media contents on the hard disk
Do you want to continue (Y or N)
```

14 Hard Disk Random Seek Test. This test does random seek tests in between head selects. Verifies the entire hard disk drive. In the first part of this test, you are asked to select the drive that is to be tested. The second option asks whether autoflag is to be used:

```
Enter autoflag selection or <Esc> to exit.
(0) Disable autoflag.
(1) Enable autoflag.
```

About Autoflag: The Hard Disk Random Seek Test, Hard Disk Write/Read Test, and Hard Disk Verify Test each include the autoflag option. Only the hard-disk tests in the field-service diagnostics (FDX) have the autoflag option. The hard-disk tests in the system-confidence diagnostics do not have the autoflag option. Autoflag updates the bad sector tables on the hard drive with the locations of sectors having hard errors or repeated soft errors.

The hard-disk tests check the hard drive for bad sectors. Unflagged bad sectors, or new bad sectors on the hard disk are detected by one of three different error conditions:

1. Record Not Found Error (RNF error)
2. ECC (ECC error)
3. Data Address Mark (DAM error)

The diagnostic test retries a failing bad sector up to 16 times. The error is then categorized as a hard or a soft error. Soft errors are recovered within 16 retries, hard errors are not. A soft error occurring twice within two loops is treated as a hard error.

If autoflagging is enabled in the hard drive tests, the bad sector table is updated with the absolute sector number of the failing bad sector. The absolute sector number corresponds to the track, head, and sector number of each sector on the hard drive. Each sector of the hard drive has an absolute sector number, so that the bad sector table can keep track of the bad sectors on the hard disk.

The bad sector table stores a 32-bit long word that designates the absolute sector numbers. The absolute sector number partitions the drive into incremental 512 blocks that can be accessed. The first and last hard disk locations and the absolute sector numbers that identify them are as follows:

Hard Drive	Location	Absolute Sector Number
Track 0	head 0 sector 0	000000
Track 1023	head 8 sector 15	131072

The hard drive bad sector tables are updated with the absolute sector number of unflagged or new bad sectors when autoflag is enabled. The bad sector table information is contained in two locations, track 0 and the maximum outermost track on the hard drive.

Track 0 sectors zero, six and seven contain a copy of the main drive configuration table and the bad sector table. A duplicate copy of the same information resides on the maximum track and maximum head in the first usable three sectors.

This duplication of the drive configuration and bad sector information on two different locations on the hard drive reduces the likelihood of losing the drive. If the operating system gives error messages indicating fatal hard drive problems and the field service engineer suspects that the problems is caused by new or unflagged bad sectors, the hard disk tests should be run with autoflag enabled.

After the diagnostics have run, the operating system can be immediately reinstalled.

The Hard Disk Random Seek Test lists the number of hard and soft errors at the end of the test. Three retries are allowed. Error messages for this test show the drive, head, track, and sector number of any soft or hard errors. Also, FDL errors are listed along with the pass of the test that they occurred on. If the test runs without error , a series of dots are displayed on the screen, followed by a message that the hard disk random seek test has passed.

15 Hard Disk Verify Test. In this test, the head, cylinder, and sector number on each drive in the system is verified. In the first part of this test, you are asked to select the drive that is to be tested.

16 Systems Test. Tests the floppy disk drive, hard disk drive, and memory in three parts. This is a destructive test that overwrites all existing data on the tape, floppy disk, and hard disk.

The first part of this test is as follows:

1. The test program begins by writing a one sector of test data from system memory to both the hard and floppy disk.

2. The test then writes the test data into two separate 512 byte test locations in physical memory.

3. The CPU compares the contents of these test locations. The test passes if they match, and an error message is displayed if they do not.

The above steps occur concurrently, and are repeated for each sector on the floppy disk. This process is called "working double buffer pairs through memory". Testing is done on a floppy's worth of data on the hard disk (heads 0 and 1, tracks 0 through 79, 9 sectors) and on the entire floppy disk (tracks 0 through 79).

The second part tests the entire hard disk using ROM data as a test pattern. First, the hard disk is written track-by-track with a test pattern, then each track is read back and verified.

The third part tests the streaming tape drive. The test begins by rewinding the tape to the beginning, erasing the tape, and seeking back to the beginning of the tape. Next, 512 blocks of test data are written on the tape, followed by a file mark. The tape is then rewound, and the 512 blocks of test data are read back, and checked for errors.

In the next loop of the systems test, the tape test writes and reads to the section of tape beyond the original 512 blocks that were tested. The process is repeated until the entire tape has been tested. By passcount 10 the entire tape has been tested, and the test begins at the beginning of the tape again.

Error messages include the same error messages as in the floppy, and hard disk drive tests including drive not ready and CRC errors. In addition, memory parity errors and buffer compare errors are listed.

17 Tape Append Test. This test destroys tape data. The test first seeks to the beginning of the tape, then erases the tape. Next, the test writes 1 block of test data and a file mark. Then, the test writes another 1 block of test data and goes back to verify the filemark.

18 Tape Write/Read Test. Tests the streaming tape drive (and cartridge) using all nine tracks. A message appears to warn you that this test destroys data. Then, you are asked to select the size of the streaming tape that is to be tested.

19 Floppy Random Seek Test. Verifies that the floppy disk drive is working.

The Floppy Random Seek Test does 100 seeks and lists the number of cylinder and head errors at the end of the test. Three retries are allowed. Error messages for this test list the number of seek errors, but not the location of the errors. The high-speed floppy disk can be tested by using the Parameter Menu.

20 Floppy Write/Read Test. Determines if the floppy disk drive can transfer data correctly. To run this test you need a formatted scratche disk. This test destroys any data on the floppy disk. At the start of this test you must select the speed of the drive to be tested:

```
Enter the floppy drive speed or ESC to exit:
(A) Low Speed          (B) High Speed
```

You can also run this as a read-only test by pressing **n** in reply to the prompt at the start of this test:

```
Do you wish to write on the media? (y or n)
```

If the test fails, the error message gives the failing cylinder, head, and sector. The data pattern that was expected to be found, and the data pattern that was actually found is also listed.

SIO Test Menu

Perform the following procedure to obtain the SIO Test Menu:

1. Press **n** and note that the third menu displayed is the SIO Test Menu:

```
SIO Test Menu

Test #  Description                    Status

21      SIO Checksum Test              Enabled
22      SIO Memory Test                Enabled
23      SIO LSI Chip Test              Enabled
24      SIO Internal Loopback Test     Enabled
25      SIO Barber Pole Test           Enabled
26      SIO Echo Test                  Enabled
27      SIO External Loopback Test     Enabled
28      SIO Interrupt Test             Enabled
29      SIO DMA Test                   Enabled
30      SIO WorkNet Test               Enabled
31      SIO Timer Test                 Enabled
N       Display Next Test Menu
R       Return to Field Service Menu

Enter test numbers, separated by commas, followed by <Retn>
Press <Retn> to execute all tests
Press <Esc> for next test or <Del> to exit testing

Enter:
```

2. Type the appropriate command from the SIO Test Menu to perform the following tests:

   21 SIO Checksum Test. Checks whether the 8086 can execute the code out of local memory. During this test the PROMs are summed separately so that the individual failing PROM can be isolated. A PROM failure is considered a major failure since the integrity of the firmware is in doubt.

NOTE

You should test the ports at various baud rates in tests 21, 22, and 24. To change the baud rate, obtain the Field Diagnostics Executive Menu and select the **p** (parameter) command as described under "Field Diagnostics Executive Menu." Then follow the procedure for changing the SIO parameters.

22 SIO Memory Test. Tests the 16K x 4 bit local dynamic RAM memory and refresh on the communications board. A data pattern of 5555h is written into memory and verified. Then a data pattern of AAAAh is written into memory and verified. Finally, parity is checked by toggling the parity bit through the memory.

23 SIO LSI Chip Test. Ports 0 to port 9 of the SCC integrated circuits (ICs), the DMA IC and the CIO IC registers are tested to see whether they can be accessed (except the port where the modem is connected).

24 SIO Internal Loopback Test. Alternates data patterns between 00 and FF, and uses 256 bytes of the above data patterns to test the selected port internal loopback mode at a default baud rate setting of 9600. The maximum number of errors using this method is 511 errors. If you receive this error count, the internal SIO circuitry is not working.

25 SIO Barber Pole Test. Runs a complete set of characters across the terminal screen. This test requires you to connect a terminal to the port that you wish to test. If the test is running correctly, the complete character set streams continuously across the terminal screen. Watch the test carefully for the character set to be complete.

There are no error messages in this test; if there is a hardware problem, the test will not run.

26 SIO Echo Test. Echos whichever character is typed in at a baud rate of 9600. This test also requires you to hook up a terminal to the port that you wish to test. The following message is displayed on the console:

```
Test SIO Board x

Please enter SIO port number (0 - 9) or press <Esc> to exit
```

3. Enter SIO port number and the following message is displayed on the console:

```
Press <Esc> on console and/or test port to quit the test,
press <Ctrl-a> on console to show the test port status on console
```

4. Note that **Enter:** appears on the terminal connected to the test port. Type any test characters on the test terminal and press Ctrl-a on the console. The following display appears:

```
Character(s) received: <Cr>
Character(s) not received: <Bs><Tab><Lf><Space>
```

All the characters and functions received (typed in) are displayed after the **Characters(s) received:** message. The remaining available characters and functions are displayed after the **Characters(s) not received:** message.

27 SIO External Loopback Test. This test requires the use of a loopback connector which connects the DTR/DSR and Tx/Rx data signals as the following prompt informs you:

```
Please plug in a loopback connector before running this test.
```

See **Loopback Connectors** - Appendix C for the loopback connector assembly instructions. This test checks the handshake signals, then transmits and verifies 512 bytes through a selected port. An error count is kept and the maximum number of failures is 510.

28 SIO Interrupt Test. Checks the ability of the SIO IC group to respond to different levels of interrupt priorities. Specifically, the SIO Rxbuf received interrupt, the SIO Txbuf empty interrupt, the SIO ext/status interrupt and timer A,B,C interrupt are each tested.

If the test passes, then the flag is greater than zero. But if the test fails, then the flag equals zero. The failed interrupt will be displayed, as well as the port location at which it failed.

29 SIO DMA Test. Uses port 7 in full duplex, internal loopback mode. The DMA IC uses two channels of its four channel capability to first transmit, then receive, a test data pattern. Channel 3 transmits the data, and channel 2 receives the data back from the SCC.

The test data pattern increments between 00 and FF four times with 256 bytes of test data. The test data is stored in local memory by the DMA IC. Two buffers are used to compare and verify that the test data patterns were transferred correctly. The test also verifies that the DMA end-of-process (EOP) interrupt is working correctly.

Error messages in this test state that data was transmitted but not received. Other error messages are less complete. For example, if an address pin of the DMA address latch is open, the following error message is displayed:

```
Testing...  Local Parity Error
```

And then the system locks up. Reboot (reset) the system to continue these tests.

30 SIO WorkNet Test. Tests the ability of port 9 to handle asynchronous and synchronous data link control (SDLC) data transmissions via RS-422. This port must work correctly for the local area network (LAN) to function. Disconnect the WorkNet cable, if one is connected, as the displayed prompt informs you:

```
Please disconnect the WorkNet cable (if connected)
before running this test.
Press <Cr> when ready:
```

This test consists of two parts. In the first part, external clock circuitry clocks data out of port 9 at 1.42 MHz and the asynchronous data transmission mode is tested.

In the second part, an internal clock for port 9 clocks data out at 38.4 kHz and the SDLC data transmissions are tested.

The error messages in this test show the first test as a high-speed test and the second test as a low-speed test. Error messages also give compare error (CMP) messages and framing errors (a SCC error message in which the SCC internally detects a wrong bit within a SDLC message format). For example, if the ANETCLK buffer (LS125) is removed from the SIO communications board, the SIO WorkNet Loopback Test fails, and the following error message appears:

```
High speed:  TX empty out = 256
```

Or another example: If the the ANETD lines were grounded, the following error message appears:

```
High speed:  CMP err = 765, framing err = 258, received
char Tout = 95

Low speed :  receive char Tout = 255
```

31 SIO Timer Test. Tests the parallel input/ output device as well as the internal timers. The error message for this test might be:

```
SIO Timer Registers Write/Read Error
                or
SIO Timer Count Down Error
```

File Processor Board Level Test Menu

Perform the following procedure to obtain the File Processor Board Level Test Menu (refer to Table 4-4 for the file processor and controller circuit level error messages and their probable causes):

1. Press **n** and note that the last menu displayed is the File Processor Board Level Test Menu:

```
File Processor Board Level Menu


Test #  Description                          Status

32      Hard Disk Controller Chip Test       Enabled
33      File Processor SCSI Chip Test        Enabled
34      File Processor Timer Test            Enabled
35      File Processor PROM Checksum Test    Enabled
36      Parallel Printer Port Loopback Test  Enabled
37      Tape Controller Chip Test            Enabled
38      File Processor Interrupt Test        Enabled
39      SCSI Ping Pong Buffer Test           Enabled
40      SCSI DMA Burst Logic Test            Enabled
N       Display Next Test Menu
R       Return to Field Service Menu

Enter test numbers, separated by commas, followed by <Retn>
Press <Retn> to execute all tests
Press <Esc> for next test or <Del> to exit testing

Enter:
```

2. Type the appropriate command from the File Processor and Controller Circuit Level Test Menu to perform the following tests:

   32 Hard Disk Controller Chip Test. This test has two parts. The first part writes an 01 data pattern into the registers of the Western Digital 2010 IC. Then, the pattern is read back and compared to ensure that the two patterns match.

   The pattern is rotated and the previous procedure is repeated for all possible bit positions in the pattern.

   The second part tests the drive select circuitry. The first part of this test involves attempting to select non-existent drive 3. If the status shows any drive selected, an error will be displayed showing that drive as being selected. The test then tries to select an installed drive, and gives an error message if any other drive was mistakenly selected.

33 File Processor SCSI Chip Test. Tests the 5385E SCSI protocol controller on the file processor board. First the 5385E is reset, and then the status of the diagnostic status register is read. The 5385E SCSI protocol controller must pass its internal power-up tests which include: (1) attempting an unconditional branch, (2) setting and resetting the data register full status bit in the interrupt register, (3) testing initial conditions and initial command registers, (4) resetting the internal diagnostic flag, and (5) flushing several bytes of data through the data paths of the IC.

If the previous sequence of tests passes, the test goes on to try writing and then reading data patterns of 55 and AA into the data registers.

34 File Processor Timer Test. Tests the file processor timing with the following messages:

```
checking channel 0 counter for all bits on...

checking channel 0 counter for all bits off...

checking that channel 0 doesn't count too slow

checking that channel 0 doesn't count too fast
```

35 File Processor PROM Checksum Test. Sums the PROMS in the file processor PCB, and checks for correct checksums.

36 Parallel Printer Port Loopback Test. This test requires a printer port loopback connector to be placed over the loopback port as the following prompt indicates:

```
Checking data strobe (logic high) to acknowledge...
Checking input prime* (logic low) to printer status acknowledge
```

This test checks the printer port signals using the loopback connector to loop back the signals so they can be read. See **Loopback Connectors** - Appendix C for instructions on assembling the parallel printer loopback connector.

If you do not connect a loopback connector, the test fails with the following error message:

```
ERROR:  input prime* or status acknowledge stuck high
```

37 Tape Controller Chip Test. Initializes the tape LSI controller, then resets, and the status of the controller board is read. The test begins with the following prompt:

```
Sending reset to the tape controller.
```

If this process is working correctly you should hear the streaming tape unit reset. If an error was detected, an error message will be displayed, and if not the test will continue.

Next, the test sends a self test command 1 to the tape controller. Self test 1 consists of four parts: (1) LSI controller chip test, (2) 16K RAM chip buffer test, (3) data separator logic test, and (4) 8155 PIA chip test.

38 File Processor Interrupt Test. Saves the firmware interrupt vectors and installs the test routine vectors. Next, the first interrupt to be tested is the channel 0 interrupt vector followed by the hard disk, SCSI, tape, DMA, and floppy interrupt.

Each of these interrupts must have been successfully acknowledged as the test results indicate. At the end of the test, the firmware interrupt vectors are reinstalled and the test is finished.

39 SCSI Ping Pong Buffer Test. Tests a pair of sector buffers for the ability to handle hard disk and SCSI traffic. The ping-pong buffer's principle advantage is its capacity to

provide continuous data transfer by allowing one buffer to load while the other is unloading data.

This test consists of two parts. First, a 512- word data pattern is set up in system memory and a DMA transfer is performed from the system memory to the ping-pong buffer.

If an error occurs, a message is displayed and the test stops. Then the system memory segment is cleared.

Next, a SCSI-done (SCSIDONE) signal is issued to reset the buffer sequencer. A DMA transfer is performed from the ping-pong buffer to system memory. The contents of system memory is verified with the original 512-word data pattern.

40 SCSI DMA Burst Logic Test. Verifies the ability of the burst logic circuitry to limit the file processor's use of the system bus. This test consists of two parts. First, a 512-word DMA transfer is performed with the burst logic disabled from system memory to the ping-pong buffer. If an error occurs, a message is displayed and the test stops. Then the system memory segment is cleared.

Next, a DMA transfer is performed, with the burst logic enabled, from the ping-pong buffer to system memory. The burst-on time is set for 64 words and the transfer is terminated after one burst on/off cycle. The contents of system memory is verified to be a pattern with the same length as the burst-on time.

Multidrop Communications (MDC) Test Menu

Perform the following procedure to obtain the MDC Test Menu (refer to Table 4-5 for the multidrop communications error messages and their probable causes):

1. Press **n** and note that the next menu displayed is the MDC Test Menu:

```
MDC Test Menu

Test #  Description                          Status

41      MDC PROM Checksum Test               Enabled
42      MDC System Bus Addressability Test   Enabled
43      MDC Memory March and Refresh Test    Enabled
44      MDC LSI Chips Access Test            Enabled
45      MDC Interrupt Test                   Enabled
46      MDC DMA Test                         Enabled
47      MDC WorkNet Loopback Test            Enabled
48      MDC Multidrop Loopback Test          Enabled
49      MDC Timer Test                       Enabled
50      MDC Baud Rate Test                   Enabled
51      MDC External Loopback Test           Enabled
52      MDC Internal Loopback Test           Enabled
53      MDC Barber Pole Test                 Enabled
54      MDC Echo Visual Verification Test    Enabled
55      TCU-8 External Loopback Test         Enabled
N       Display Next Test Menu
R       Return to Field Service Menu

Enter test numbers, separated by commas, followed by <Retn>
Press <Retn> to execute all tests
Press <Esc> for next test or <Del> to exit testing

Enter:
```

2. Type the appropriate command from the MDC Test Menu to perform the following tests:

   41 MDC PROM Checksum Test. During this test the PROMs are summed separately so that the individual failing PROM can be isolated. A PROM failure is considered a major failure since the integrity of the firmware is in doubt.

NOTE

You should test the ports at various baud rates in tests 51, 52, and 53. To change the baud rate, obtain the Field Diagnostics Executive Menu and select the **p** (parameter) command as described under "Field Diagnostics Executive Menu." Then follow the procedure for changing the MDC parameters.

42 MDC System Bus Addressability Test. Tests the main memory from 512K to 768K bytes (8000h to BFFFh). Also tests accesses through the system page register.

43 MDC Memory March and Refresh Test. Tests the local dynamic RAM memory and refresh on the multidrop communications PCB. First, a data pattern of 5555h is written into memory and verified. Then a data pattern of AAAAh is written into memory and verified. Then, the refresh circuitry is checked by writing a bit pattern to the memory and halting the 80286 CPU for two minutes. Then, the memory is read and compared with the expected data pattern.

44 MDC LSI Chips Access Test. Performs a write/ read test to all the LSI integrated circuit registers. The SCC, CIO, ADMA, and 8259 PIC integrated circuits are tested to see whether they can be accessed.

45 MDC Interrupt Test. Checks the ability of the MDC IC group to respond to different levels of interrupt priorities. Specifically, the SCC Rxbuf received, Txbuf empty, ext/status, timer A,B,C interrupts, and ADMA channel 0,1,2, and 3 are each tested.

If the test passes, then the flag is greater than zero. But if the test fails, then the flag equals zero. The failed interrupt will be displayed, as well as the port location at which it failed.

46 MDC DMA Test. Tests the 82258 ADMA. The ADMA is operated in the remote and fix-priority modes. Two buffers are used to compare and verify that the test data patterns were transferred correctly. Error messages in this test state that data was transmitted but not received.

47 MDC WorkNet Loopback Test. Tests the ability of port 4 to handle asynchronous and synchronous data link control (SDLC) data transmissions via RS-422. This port must work correctly for the local area network (LAN) to function. Disconnect the WorkNet cable, if one is connected, as the displayed prompt informs you:

```
Please disconnect the WorkNet cable (if connected)
before running this test.
Press <Retn> when ready:
```

This test consists of three parts. In the first part, external clock circuitry clocks data out of port 4 at 0.75M bits per second and the asynchronous data transmission mode is tested. In the second part, an internal clock for port 4 clocks data out at 1.4M bits per second and the asysnchronous data transmissions mode is tested.

In the last part, a SDLC frame is transmitted out of port 4 at 9600 baud and the SDLC mode is tested.

The error messages in this test show the first test as a high-speed test and the second test as a low-speed test. Error messages also give compare error (CMP) messages and framing errors (a SCC error message in which the SCC internally detects a wrong bit within a SDLC message format). For example, if the ANETCLK buffer (LS125) is removed from the MDC board, the MDC WorkNet Loopback Test fails, and a corresponding error message appears.

48 MDC Multidrop Loopback Test. Tests the ability of the multidrop port to handle asynchronous and synchronous data link control (SDLC) data transmissions via RS-422. This port must work correctly for the local area network (LAN) to func-

tion. Disconnect the multidrop cable, if one is connected, as the displayed prompt informs you:

```
Please disconnect the Multidrop cable (if connected)
before running this test.
Press <Retn> when ready:
```

This test consists of two parts. In the first part, external clock circuitry clocks data out of the multidrop port at 1.4M bits per second and the asynchronous data transmission mode is tested. In the second part, a SDLC frame is transmitted at 9600 baud through the multidrop port and the SDLC data transmissions are tested.

The error messages in this test show the first test as a high-speed test and the second test as a low-speed test. Error messages also give compare error (CMP) messages and framing errors (a SCC error message in which the SCC internally detects a wrong bit within a SDLC message format).

For example, if the ANETCLK buffer (LS125) is removed from the MDC PCB, the MDC Multidrop Loopback Test fails, and a corresponding error message appears.

49 MDC Timer Test. Writes/reads and verifies the CIO registers. Starts and stops the A, B, and C timers to verify that the timers are working. Also, checks the timer interrupts.

50 MDC Baud Rate Test. Tests SCC Tx and Rx baud rate using the CIO timer.

51 MDC External Loopback Test. This test requires the use of a loopback connector which connects the DTR/DSR and Tx/Rx data signals as the following prompt informs you:

```
Please plug in a loopback connector(s) before running this test.
```

Refer to **Loopback Connectors** - Appendix C for the loopback connector assembly instructions. This test performs the following:

- transmits and receives 512 bytes of data
- checks the CTS/RTS handshake signals
- compares received and transmitted characters
- checks for receiver timeout
- checks Sync signal for ports 2 and 3

52 MDC Internal Loopback Test. Alternates data patterns between 00 through FF, and uses 512 bytes of the above data patterns to test the multidrop port internal loopback mode at a default baud rate setting of 9600. The maximum number of errors using this method is 511. If you receive this error count, the internal MDC circuitry is not working. This test also compares received and transmitted characters and checks for receiver timeout.

53 MDC Barber Pole Test. Runs a complete set of characters across the terminal screen. This test requires you to connect a terminal to the port that you wish to test. If the test is running correctly, the complete character set streams continuously across the terminal screen. Watch the test carefully for the character set to be complete. There are no error messages in this test; if there is a hardware problem, the test will not run.

54 MDC Echo Visual Verification Test. Echos whichever character is typed in at a baud rate of 9600. This test also requires you to hook up a terminal to the port that you wish to test. There are no error messages in this test; if there is a hardware problem, the test will not run. The following message is displayed:

```
Test MDC Board x

Please enter MDC port number (0 - 9) or press <Esc> to exit
```

3. Enter MDC port number and the following message is displayed on the console:

```
Press <Esc> on console and/or test port to quit the test.
press <Ctrl-a> on console to show the test port status on console
```

4. Note that **Enter:** appears on the terminal connected to the test port. Type any test characters on the test terminal and press Ctrl-a on the console. The following display appears:

```
Character(s) received: <Cr>
Character(s) not received: <Bs><Tab><Lf><Space>
```

All the characters and functions received (typed in) are displayed after the **Characters(s) received:** message. The remaining available characters and functions are displayed after the **Characters(s) not received:** message.

55 TCU-8 External Loopback Test. Tests the network protocol between the MDC board and the TCU-8(s). Transmits a block of data to the selected secondary station, receives the data back, and verifies. Requires a loopback connector that connects the DSR/DTR and Tx/Rx data lines together. Refer to **Loopback Connectors** - Appendix C for loopback connector assembly instructions.

Tables 4-1 through 4-5 list the field diagnostics executive (FDX) tests, related error messages, and their probable cause.

NOTE

The following unexpected NMI error messages can appear while performing any of the CPU and system memory tests.

CPU::Error 46 : Unexpected NMI - CPU MRD Parity error

CPU::Error 47 : Unexpected NMI - CPU Bus Timeout :CPU

CPU::Error 48 : Unexpected NMI - CPU Bus Timeout :MEM

CPU::Error 49 : Unexpected NMI - CPU Bus Timeout :I/O

CPU::Error 50 : Unexpected NMI - UPS

CPU::Error 51 : Unexpected NMI - CPU MRD Parity error & UPS

CPU::Error 52 : Unexpected NMI - CPU Bus Timeout :CPU & UPS

CPU::Error 53 : Unexpected NMI - CPU Bus Timeout : MEM & UPS

CPU::Error 54 : Unexpected NMI - CPU Bus Timeout : I/O & UPS",

CPU::Error 66 : Unexpected NMI - UNKNOWN SOURCE

Table 4-1. CPU and System Memory FDX Trouble Analysis

Test	Error Message	Probable Cause
(1) CPU PROM Checksum	**CPU::Error 01 : EPROM-checksum error (even PROM)\0** **CPU::Error 02 : EPROM-checksum error(odd PROM)\0**	**NOTE** The following CPU error messages are self-explanatory. No probable causes are included here.
(2) CPU MMU/ALU	**CPU::Error 69 : Paging mechanism Failure of 80386 CPU** **CPU::Error 70 : 32 bit multiply failure of 80386 CPU - BAD PART!!** **CPU::Error 71 : 16 bit multiply failure of 80386 CPU - BAD PART!!** **CPU::Error 37 : 80386 CPU - Unable to Multi-Task** **CPU::Error 38 : 80386 CPU - Handling exception 6 incorrectly** **CPU::Error 39 : 80386 CPU - Illegal Exception occurred**	

Table 4-1. CPU and System Memory FDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
(3) CPU Cache RAM	CPU::Error 40 : CACHE RAM - Set 0 data ripple failure	
	CPU::Error 41 : CACHE RAM - Set 1 data ripple failure	
	CPU::Error 42 : CACHE RAM - Set 0 address ripple failure	
	CPU::Error 43 : CACHE RAM - Set 1 address ripple failure	
	CPU::Error 44 : CACHE RAM - Set 0 content failure	
	CPU::Error 45 : CACHE RAM - Set 1 content failure	
(4) CPU Bus Size RAM	CPU::Error 16 : Bus Size RAM- Data ripple failure	
	CPU::Error 17 : Bus Size RAM- Address ripple failure	
	CPU::Error 18 : Bus Size RAM- Content failure	

Table 4-1. CPU and System Memory FDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
(5) CPU Cacheable Page RAM	CPU::Error 30 : Cacheable Page RAM- Data ripple failure	
	CPU::Error 31 : Cacheable Page RAM- Address ripple failure	
	CPU::Error 32 : Cacheable Page RAM- Content failure	
(6) CPU Tag RAM	CPU::Error 27 : TAG RAM- Data ripple failure	
	CPU::Error 28 : TAG RAM- Address ripple failure	
	CPU::Error 29 : TAG RAM- Content failure	
(7) CPU CIO	CPU::Error 19 : CIO - Initialization failure	
	CPU::Error 20 : CIO - Port C error	
	CPU::Error 21 : CIO - Data ripple failure	
	CPU::Error 22 : CIO - Counter(s) not counting	

Table 4-1. CPU and System Memory FDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
(7) CPU CIO (Cont.)	CPU::Error 23 : CIO - Incorrect counting for counters	
(8) CPU PIC Interrupt	CPU::Error 33 : PIC 8259 - Register read write failure	
	CPU::Error 34 : PIC/ CIO - Interrupt 6 mechanism malfunction	
	CPU::Error 35 : PIC/ CIO - Interrupt 5 mechanism malfunction	
	CPU::Error 36 : PIC/ CIO - Interrupt 0 mechanism malfunction	
(9) CPU Real Time Clock	CPU::Error 06 : RTC-Battery/NV RAM test failure occurred	
	CPU::Error 24 : RTC - Data ripple failure	
	CPU::Error 25 : RTC - Address ripple failure	
	CPU::Error 26 : RTC - Content failure	

Table 4-1. CPU and System Memory FDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
(10) CPU Cache Functional	CPU::Error 55 : CACHE RAM Functional - Cache Write Miss failure	
	CPU::Error 56 : CACHE RAM Functional - Cache Read Miss failure	
	CPU::Error 57 : CACHE RAM Functional - Cache Read Miss Tags failure	
	CPU::Error 58 : CACHE RAM Functional - Cache Write Hit failure",	
	CPU::Error 59 : CACHE RAM Functional - Cache Read Hit failure	
	CPU::Error 60 : CACHE RAM Functional - Forced Cache write Miss failure	
	CPU::Error 61 : CACHE RAM Functional - Tag invalidation failure	
	CPU::Error 62 : CACHE RAM Functional - Cache set 0 Unable to CACHE --IN\r\n data while executing locally	
	CPU::Error 63 : CACHE RAM Functional - Cache set 1 Unable to CACHE --IN\r\n data while executing locally	

Table 4-1. CPU and System Memory FDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
(10) CPU Cache Functional (Cont.)	CPU::Error 64 : CACHE RAM Functional - Cache set 0 unable to execute code\r\n out of cache	
	CPU::Error 65 : CACHE RAM Functional - Cache set 1 unable to execute code\r\n out of cache	
(11) CPU 80387 Numeric Processor	CPU::Error 67 : The 80387 device is absent	
	CPU::Error 68 : The 80387 device is present	
	CPU::Error 07 : Numeric Processor- initialization error	
	CPU::Error 08 : Numeric Processor- Packed Decimal division error	
	CPU::Error 09 : Numeric Processor- Packed Decimal addition error	
	CPU::Error 10 : Numeric Processor- Packed Decimal subraction error	
	CPU::Error 11 : Numeric Processor- Packed Decimal multiplication error	
	CPU::Error 12 : Numeric Processor- Illegal exch-ange in NPX Stack	

Table 4-1. CPU and System Memory FDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
(11) CPU 80387 Numeric Processor (Cont.)	CPU::Error 13 : Numeric Processor- Incorrect square root in NPX Stack	
	CPU::Error 14 : Numeric Processor- Floating point add/subract incorrect	
	CPU::Error 15 : Numeric Processor-Floating point multiply/divide incorrect	
(12) Memory	CPU::Error 03 : Memory-Hole detected. Check memory pinning	
	CPU::Error 04 : Memory-Parity error detected	
	CPU::Error 05 : Memory-Compare error occurred	
	CPU::Error 72 : Download failed in Bus Arbitration test	
	CPU::Error 73 : Execute command failed in Bus Arbitration test	
	CPU::Error 74 : System Bus Arbitration failed	

Table 4-2. File Processor and Controller FDX Trouble Analysis

Test	Error Message	Probable Cause
(13),(14), (15) Hard Disk Random Seek, Read/ Write and Verify	**Cannot write configuration table to drive x cylinder x head x sector x**	• Hard disk • Circuitry between DP8466 and hard disk • WRGATE not present
	Compare error expecting xxxx receiving xxxx x words into buffer on drive x cylinder x head x sector x	• Hard disk • Circuitry between DP8466 and DMA controller • System memory
	Cannot read configuration table on drive x cylinder x head x sector x	• Hard disk • Read data or RDCLK not present • DP8466 (3C) • File processor or controller data transceiver (3H) • Multibus buffer transceivers on file processor (5F, 5H) • System memory
	Could not seek to drive x cylinder x head x sector x	• Hard disk • DP8466 (3C) • File processor or controller data transceiver (3H) • Multibus buffer transceivers on file processor (5F, 5H) • System memory

Table 4-2. File Processor and Controller FDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
(13),(14), (15) Hard Disk Random Seek, Read/ Write and Verify (Cont.)	**Can't read bad sector table on drive x cylinder x head x sector x**	• Hard disk • Read data or RDCLK not present • DP8466 (3C) • File processor or controller data transceiver (3H) • Multibus buffer transceivers on file processor (5F, 5H) • System memory
	Can't flag drive x cylinder x head x sector x	• Hard disk - media defect or logic • Read data or RDCLK not present • DP8466 (3C) • File processor or controller data transceiver (3H) • Multibus buffer transceivers on file processor (5F, 5H) • System memory
	RNF on drive x cylinder x head x sector x	• Hard disk - media defect or logic • Read data or RDCLK not present • DP8466 (3C) • File processor or controller data transceiver (3H) • Multibus buffer transceivers (5F, 5H) on file processor

Table 4-2. File Processor and Controller FDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
(13),(14), (15) Hard Disk Random Seek, Read/ Write and Verify (Cont.)	**ECC on drive x cylinder x head x sector x**	• Hard disk - media defect or logic • Read data or RDCLK not present • DP8466 (3C) • File processor or controller data transceiver (3H) • Multibus buffer transceivers (5F, 5H) on file processor • System memory
	DAM on drive x cylinder x head x sector x	• Hard disk - media defect or logic • Read data or RDCLK not present • DP8466 (3C) • File processor or controller data transceiver (3H) • Multibus buffer transceivers (5F, 5H) on file processor • System memory

Table 4-2. File Processor and Controller FDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
(13),(14), (15) Hard Disk Random Seek, Read/ Write and Verify (Cont.)	**Cannot read drive x cylinder x head x sector x**	• Hard disk - media defect or logic • Read data or RDCLK not present • DP8466 (3C) • File processor or controller data transceiver (3H) • Multibus buffer transceivers (5F, 5H) on file processor • System memory
	Cannot format drive x cylinder x head x sector	• Hard disk - media defect or logic • Circuitry between DP8466 and hard disk
	Excessive retries = x HARD drive x	• Hard disk - media defect or logic • Read data or RDCLK not present • DP8466 (3C) • File processor or controller data transceiver (3H) • Multibus buffer transceivers (5F, 5H) on file processor • System memory

Table 4-2. File Processor and Controller FDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
(13),(14), (15) Hard Disk Random Seek, Read/ Write and Verify (Cont.)	**Excessive seek errors on HARD drive x**	• Hard disk - media defect or logic • Circuitry between DP8466 and hard disk • WRGATE not present
	Retry table overflow. Error count greater than 2x	• Retries exceeded software limit • Hard disk - media defect or logic • Read data or RDCLK not present • DP8466 (3C) • File processor or controller data transceiver (3H) • Multibus buffer transceivers (5F, 5H) on file processor • System memory
	Cannot initialize the HARD disk controller	• Hard disk • DP8466 (3C) • Controller board status port (8E) • 8086 circuitry on file processor board • File processor RAM
	Sector Header Error Expected drive x track x head x sector x Recieved drive x track x head x sector x	• Hard disk • Backplane hard disk termination • DP8466 (3C)

Table 4-2. File Processor and Controller FDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
(13),(14), (15) Hard Disk Random Seek, Read/ Write and Verify (Cont.)	**Can't read backup drive configuration table on track x head x**	• Hard disk - media defect • DP8466 (3C) • Disk formatted with previous version of diagnostics (ST-506 only)
	Can't read backup bad sector table on track x head x	• Hard disk - media defect • DP8466 (3C) • Disk formatted with previous version of diagnostics (ST-506 only)
	Drive ready does not go false for illegal drive x	• Hard disk • LED board • LS 240 (9C) • 38 (14D)
	Expected data xxxx and received xxxx x words into buffer from HARD	• Hard disk • Read data or RDCLK not present • DP8466 (3C) • File processor or controller data transceiver (3H) • Multibus buffer transceivers on file processor (5F, 5H) • System memory
	There are no drives ready for test	• Hard disk • LED board • LS 240 (9C) • 38 (14D)

Table 4-2. File Processor and Controller FDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
(16) System	File processor reports cartridge not in place on TAPE drive x	• Cartridge not installed or improperly installed
	File processor reports unrecoverable data error on TAPE drive x	• Perform tests 17 & 18
	File processor reports tape is write protected on TAPE drive x	• Perform tests 17 & 18
	File processor reports end of media on TAPE drive x	• Streaming tape drive
	File processor reports no data on tape on TAPE drive x	• Streaming tape drive • Perform tests 17 & 18
	File processor reports illegal command issued on TAPE drive x	• ALS 3T4 (27E) • ALS 273 (27D) • 8031 (27A)
	Could not write pattern xxxx to track 0 head 1	• Perform tests 13-15
	Could not read pattern xxxx from track 0 head 1	• Perform tests 13-15
	Could not write pattern xxxx to track 0 head 1 of the hard disk	• Perform tests 13-15
	NMI error occurred at offset xxxx in segment xxxx	• Perform tests 7 & 8

Table 4-2. File Processor and Controller FDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
(16) System (Cont.)	The data expected was xxxx and received was xxxx	• Perform tests 13-15
	Data compare expecting xxxx and receiving xxxx at location xxxx in segment xxxx	• Perform tests 13-15
	There was no compare error so check for slow ram or slow parity generator	• Perform test 12
	The data was written correctly!!! Cannot isolate with a read!!!	• Perform test 12
	Data Error - Hdata xxxx Fdata xxxx Expected xxxx	• Perform tests 12,13, 20, & 32
	Error occurred between address xxxx (Hdata) and xxxx (Fdata) in segment xxxx	• Perform tests 12,13, 20, & 32
	There was an NMI detected in segment xxxx	• Perform tests 7,8, & 12
(17),(18) Streaming Tape Write/ Read and Append	Unrecoverable data error	• Streaming tape • Tape drive • CPU 8031 tape controller (21A) • File processor DMA controller (21D)

Table 4-2. File Processor and Controller FDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
(17),(18) Streaming Tape Write/ Read and Append (Cont.)	**Cartridge is write protected**	• Streaming tape write protected
	Cartridge is not in place	• Tape drive • Tape missing
	Read error, no data detected	• Tape drive • CPU 8031 tape controller (21A)
(19) Floppy Random Seek	**Operation timeout error (DMA or INT)**	• Floppy disk • Floppy drive • Circuitry between floppy and DMA controllers
(20) Floppy Write/Read	**Compare error cyl= x, head= x, sector= x**	• Floppy disk • Floppy drive • Circuitry between floppy and DMA controllers • System memory
	(read/write) **error: cyl = x, head = x, sector = x**	• Floppy disk • Floppy drive • Circuitry between floppy and DMA controllers • System memory
	Diskette is write protected	• Protected floppy disk • Floppy drive

Table 4-3. SIO Communications FDX Trouble Analysis

Test	Error Message	Probable Cause
(21) SIO PROM Checksum	**SIO PROM checksum error Odd Checksum = xxxxh Even Checksum = xxxxh**	• SIO PROM (20C-A or 20C-B) • Address buffers (13F)
(22) SIO Memory	**SIO local memory fail at x = xh Expected Data = xxxxh Received Data = xxxxh**	• Address buffers (16F, 17F, 19E) • RAM (2J-9J, 11J-18J)
	SIO local memory parity error at x	• Memory parity (1J, 10J) • RAM (2J-9J, 11J-18J) • Address buffers (16F, 17F, 19E)
(23) SIO LSI	**SIO DMA chip registers write/read error**	• DMA controller (17D) • Address latch (13D, 15F) • Local bus control (15D, 16C, 20C, 17C)
	SIO SCC chip registers write/read error at port x (Port Address = xxxxh	• SCCs (1B, 3B-6B)
	SIO CIO chip registers write/read error at port x	• CIO (2B)

Table 4-3. SIO Communications FDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
(24) SIO Internal Loopback	Receive character time-out at the xxxx character	• SCCs (1B, 3B-6B, 1A-10A)
	Compare error = x	• SCCs (1B, 3B-6B)
(27) SIO External Loopback	RTS/CTS handshake not responding	• SCCs (1B, 3B-6B, 1A-10A) • No loopback cnctr
	Receive character time-out at the xxxx character	• SCCs (1B, 3B-6B, 1A-10A) • No loopback cnctr
	Compare error = x	• SCCs (1B, 3B-6B)
	Handshake signal changed unexpectedly xx time(s)	• SCCs (1B, 3B-6B, 1A-10A)
(28) SIO Interrupt Vector	Port x Tx interrupt fail	• SCCs (1B, 3B-6B, 1A-10A) • SIO memory (interrupt vector area)
	Port x Rx interrupt fail	• SCCs (1B, 3B-6B, 1A-10A) • SIO memory (interrupt vector area)
	Port x ext/status interrupt fail	• SCCs (1B, 3B-6B, 1A-10A) • SIO memory (interrupt vector area)
	Timer xx interrupt fail	• CIO (2B)

Table 4-3. SIO Communications FDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
(29) SIO DMA	SIO DMA Test Has Compare Errors (DMA Tx and Rx 1K Byte Data) 1. Tx Data = xxxxh Rx Data = xxxxh 2. Tx Data = xxxxh Rx Data = xxxxh	• DMA controller (17D) • SCCs (1B, 3B) • SIO memory (Rx or Tx buffers) (1A-6A)
	DMA EOP interrupt fail	• DMA controller (17B) • CIO (2B)
(30) SIO WorkNet	High speed WorkNet loop-back (transmit 768 bytes) Compare error = x	• DMA controller (17D) • SCC0 (1B) • RS-422 loopback ckt. (3A, 4A, 1C) • External clock (2E, 4E, 3D, 4C)
	High speed WorkNet Parity error=x	• DMA controller (17D) • SCC0 (1B) • RS-422 loopback ckt. (3A, 4A, 1C)
	High speed WorkNet Overrun error = x	• DMA controller (17D) • SCC0 (1B) • RS-422 loopback ckt. (3A, 4A, 1C) • External clock (2E, 4E, 3D, 4C)
	High speed WorkNet Framing error = x	• DMA controller (17D) • SCC0 (1B) • RS-422 loopback ckt. (3A, 4A, 1C) • External clock (2E, 4E, 3D, 4C)

Table 4-3. SIO Communications FDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
(30) SIO WorkNet (Cont.)	High speed WorkNet DTR timeout = x	• DMA controller (17D) • SCC0 (1B) • RS-422 loopback ckt. (3A, 4A, 1C) • Carrier sense ckt. (1D, 2D, 8D)
	High speed WorkNet Tx empty timeout = x	• DMA controller (17D) • SCC0 (1B) • RS-422 loopback ckt. (3A, 4A, 1C) • External clock (2E, 4E, 8D, 3D, 4C)
	High speed WorkNet Receive character timeout = x	• SCC0 (1B) • RS-422 loopback ckt
	Low speed WorkNet loop-back(transmit 256 bytes) CRC error = x	• SCC0 (1B) • RS-422 loopback ckt
	Low speed WorkNet Compare error = x	• SCC0 (1B) • RS-422 loopback ckt
	Low speed WorkNet Overrun error = x	• SCC0 (1B) • RS-422 loopback ckt
	Low speed WorkNet DTR timeout = x	• SCC0 (1B) • RS-422 loopback ckt • Carrier sense ckt (1D, 2D, 8D)
	Low speed WorkNet Tx empty timeout = x	• SCC0 (1B) • RS-422 loopback ckt
	Low speed WorkNet Underrrun timeout = x	• SCC0 (1B) • RS-422 loopback ckt.

Table 4-3. SIO Communications FDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
(30) SIO WorkNet (Cont.)	**Low speed WorkNet Receive character timeout = x**	• RS-422 loopback ckt. • SCC0 (Port 9) (1B)
(31) SIO Timer	**SIO timer registers write/read error**	• CIO (2B)
	SIO timer countdown error	• CIO (2B)

Table 4-4. File Processor and Controller (Circuit Level) FDX Trouble Analysis

Test	Error Message	Probable Cause
(32) Hard Disk Controller	**Verify error checking DP8466 sector count register**	• DP8466 (3C) • ALS 245 (7C, 5C) • PALs (1C, 2C) • File processor PCB
	Verify error checking DP8466 sector operation count register	• DP8466 (3C) • ALS 245 (7C, 5C) • PALs (1C, 2C) • File processor PCB
	Verify error checking DP8466 sector byte count low register	• DP8466 (3C) • ALS 245 (7C, 5C) • PALs (1C, 2C) • File processor PCB
	Verify error checking DP8466 sector byte count high register	• DP8466 (3C) • ALS 245 (7C, 5C) • PALs (1C, 2C) • File processor PCB

Table 4-4. File Processor and Controller (Circuit Level) FDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
(32) Hard Disk Controller (Cont.)	**Verify error checking DP8466 DMA address byte 0 register**	• DP8466 (3C) • ALS 245 (7C, 5C) • PALs (1C, 2C) • File processor PCB
	Verify error checking DP8466 DMA address byte 1 register	• DP8466 (3C) • ALS 245 (7C, 5C) • PALs (1C, 2C) • File processor PCB
	NOTE The following tests apply for the -002 version of the file processor board only.	
(33) File Processor SCSI Chip	**Unconditional branch failure in internal sequencer**	• SCSI controller (1C) • SCSI command or data transceivers (2B, 3A, 4A, 7A, 7B, 9A, 10A, 10C)
	Data register full bit failure in interrupt register	• SCSI controller (1C) • SCSI command or data transceivers (2B, 3A, 4A, 7A, 7B, 9A, 10A, 10C)
	Diagnostic flag failure	• SCSI controller (1C) • SCSI command or data transceivers (2B, 3A, 4A, 7A, 7B, 9A, 10A, 10C)
	Data turnaround failure	• SCSI controller (1C) • SCSI command or data transceivers (2B, 3A, 4A, 7A, 7B, 9A, 10A, 10C)

Table 4-4. File Processor and Controller (Circuit Level) FDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
(33) File Processor SCSI Chip (Cont.)	**Unused error bit setting in status register**	• SCSI controller (1C) • SCSI command or data transceivers (2B, 3A, 4A, 7A, 7B, 9A, 10A, 10C)
	SCSI chip status shows self diagnostic not complete	• SCSI controller (1C) • SCSI command or data transceivers (2B, 3A, 4A, 7A, 7B, 9A, 10A, 10C)
	SCSI auxiliary status register not reset	• SCSI controller (1C) • SCSI command or data transceivers (2B, 3A, 4A, 7A, 7B, 9A, 10A, 10C)
	Initial conditions in wrong state	• SCSI controller (1C) • SCSI command or data transceivers (2B, 3A, 4A, 7A, 7B, 9A, 10A, 10C)
	SCSI status shows command not complete	• 8259 interrupt controller (8H) • SCSI controller (1C) • SCSI interrupt line to 8259 interrupt controller • Interrupt latch or gate (25C and 4B)
	SCSI data register returned incorrect data pattern	• SCSI controller (1C) • SCSI command or data transceivers (2B, 3A, 4A, 7A, 7B, 9A, 10A, 10C)

Table 4-4. File Processor and Controller (Circuit Level) FDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
(33) File Processor SCSI Chip (Cont.)	**SCSI data register not full after completion of diagnostic command**	• 8259 interrupt controller (8H) • SCSI controller (1C) • SCSI interrupt line to 8259 interrupt controller • Interrupt latch or gate (25C and 4B)
	Internal turnaround failure with data pattern (AA/55)	• 8259 interrupt controller (8H) • SCSI controller (1C) • SCSI interrupt line to 8259 interrupt controller • Interrupt latch or gate (25C and 4B)
	SCSI chip unknown status error code	• 8259 interrupt controller (8H) • SCSI controller (1C) • SCSI interrupt line to 8259 interrupt controller • Interrupt latch or gate (25C and 4B)
	SCSI chip (initial/ final) turnaround miscompare failure	• SCSI controller (1C) • SCSI command or data transceivers (2B, 3A, 4A, 7A, 7B, 9A, 10A, 10C)
	SCSI chip turnaround bad parity failure	• SCSI controller (1C) • SCSI command or data transceivers (2B, 3A, 4A, 7A, 7B, 9A, 10A, 10C)

Table 4-4. File Processor and Controller (Circuit Level) FDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
(33) File Processor SCSI Chip (Cont.)	**Initial command bits incorrect**	• SCSI controller (1C) • SCSI command or data transceivers (2B, 3A, 4A, 7A, 7B, 9A, 10A, 10C)
	SCSI interrupt not detected	• 8259 interrupt controller (8H) • SCSI controller (1C) • SCSI interrupt line to 8259 interrupt controller • Interrupt latch or gate (25C and 4B)
(34) File Processor Timer	**Channel 0 counter failed to** (set/clear) **all bits**	• 8254 timer (25B) • Clock divider (33B)
	Channel 0 counter was too (slow/fast) **or problem with timer interrupt logic**	• 8254 timer (25B) • Clock divider (33B)
(35) File Processor PROM Checksum	**File processor** (odd/even) **checksum error**	• PROM (9H, 33D)

Table 4-4. File Processor and Controller (Circuit Level) FDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
(36) Printer Port Loopback	**Data strobe, input prime or printer status acknowledge stuck high**	• Printer port pins shorted or open • Loopback connector • Printer drivers (16A, 17A) • Printer data port (19A) • Printer status port (20A)
	Input prime * or printer status acknowledge stuck high	• Printer port pins shorted or open • Loopback connector • Printer drivers (16A, 17A) • Printer data port (19A) • Printer status port (20A)
	Printer data line (1 or 2/3 or 4/5 or 6/7 or 8) **logic** (high/low),**should be logic** (low/high)	• Printer port pins shorted or open • Loopback connector • Printer drivers (16A, 17A) • Printer data port (19A) • Printer status port (20A)
(38) File Processor Interrupt	**Timer channel 0 interrupt not detected**	• 8259 interrupt controller (8H) • 8254 timer (25B) • Interrupt line from timer to interrupt controller

Table 4-4. File Processor and Controller (Circuit Level) FDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
(38) File Processor Interrupt (Cont.)	**Hard disk interrupt not detected**	• DP8466 controller (6C) • 8259 interrupt controller (8H) • Interrupt line from DP8466 to 8259 interrupt controller (8H) on file processor PCB • Interrupt line driver (10C) on controller PCB
	Hard disk controller is busy and unable to accept a command	• DP8466 controller (6C)
	SCSI status shows self diagnostic not complete SCSI interrupt not detected	• SCSI controller (1C) • Interrupt line from SCSI controller to 8259 interrupt controller • Interrupt latches and gates (4B and 25C) on file processor PCB
	Unable to test the tape interrupt logic	• Unable to perform read tape status command

Table 4-4. File Processor and Controller (Circuit Level) FDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
(38) File Processor Interrupt (Cont.)	**Floppy disk controller interrupt not detected**	• Floppy disk controller (8C) • Interrupt line to interrupt controller from file processor to controller PCB • 8259 interrupt controller (8H) on file processor PCB
	DMA controller interrupt not detected	• 8259 interrupt controller (8H) • DMA controller (21D) • DMA interrupt line
	Hot interrupt detected	• 8259 interrupt controller (8H) on file processor PCB
	Interrupt controller mask register verify verify data = (00/FF)	• 8259 interrupt controller (8H) on file processor PCB
(39) Ping-Pong Buffer	**DMA controller operation not complete**	• DMA controller (21D) • DMA bus
	Data miscompare on transfer from ping-pong buffer	• DMA controller (21D) • Ping-pong buffer 7D, 4D, 5D, 3D, 2D, 1D 6B, 9D, 9C, 6D, 8C, 7C, 8B, 13A, 12D, 8D, 12C, 14D, 2H, 13D, 11D, 11A, 11C)

Table 4-4. File Processor and Controller (Circuit Level) FDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
(39) Ping-Pong Buffer (Cont.)	DMA error	• DMA controller (21D)
(40) DMA Burst Logic (SCSI)	Burst (on/off) logic error	• Burst logic ICs 31B, 32B, 26D) • 8254 timer controller (25B)
	DMA controller operation not complete	• DMA controller (21D)

Table 4-5. Multidrop Communications FDX Trouble Analysis

Test	Error Message	Probable Cause
(41) MDC PROM Checksum	MDC PROM Checksum Error	• PROMs (1D, 2D)
	Odd checksum = xxxx	• PROMs (1D, 2D)
	Even checksum = xxxx	• PROMs (1D, 2D)
(42) Sys-Address-ability	Data write/read error MDC system page register = xxxx MDC data address =xxxx: xxxxh Expected data = xxxxh, received data = xxxxh	• AS 534 (8E) • Incorrect jumper E6

Table 4-5. Multidrop Communications FDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
(43) MDC Memory March and Refresh	MDC local memory parity error at xxxx:xxxxh	• AS 280 (1C, 2C) • RAMs (1F-17F) • RAS/CAS control circuits
	MDC local memory fail at xxxx:xxxxh Data = xxxxh Received Data = xxxxh	• RAMs (1F-17F)
(44) MDC LSI Chips Access	MDC Timer Register Write/ Read Error CIO Register = xxxxh Expected Data = xxxxh Received Data = xxxxh	• 8536 (15B) • 8259 (20B) • 82258 (8B)
	MDC SCC Register Write/ Read Error at Port x Expected Data = xxxxh Received Data = xxxxh	• SCC • 82258 (8B)
	MDC PIC Register Write/ Read Error	• 8536 (15B) • 8259 (20B) • 82258 (8B)
	MDC DMA Register Write/ Read Error DMA Register Address = xxxxh Expected Data = xxxxh Received Data = xxxxh	• 8536 (15B) • 8258 (8B)

Table 4-5. Multidrop Communications FDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
(45) MDC Interrupt	MDC Timer x Count Down Error	• 8536 (15B) • 8259 (20B) • 82258 (8B) • SCC
	MDC Timer x Interrupt Error	• 8536 (15B) • 8259 (20B) • 82258 (8B) • SCC
	Port x Tx Interrupt Failed	• 8536 (15B) • 8259 (20B) • 82258 (8B) • SCC
	Port x Rx Interrupt Failed	• 8536 (15B) • 8259 (20B) • 82258 (8B) • SCC
	Port x Ext/Status Interrupt Failed	• 8536 (15B) • 8259 (20B) • 82258 (8B) • SCC
(46) MDC DMA	DMA channel x transmit time-out error	• DMARDY PAL (13C) • 82258 (8B) • F245 (9C-11C, 11D)
	DMA channel x End-of-DMA interrupt failed	• DMARDY PAL (13C) • 82258 (8B) • F 245 (9C-11C, 11D)
	Expected Data = xxxxh Received Data = xxxxh	• DMARDY PAL (13C) • 82258 (8B) • F245 (9C-11C, 11D)

Table 4-5. Multidrop Communications FDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
(46) MDC DMA (Cont.)	DMA subchannel x and x time-out error	• DMARDY PAL (13C) • 82258 (8B) • F245 (9C-11C, 11D)
	DMA subchannel x and x compare error	• DMARDY PAL (13C) • 82258 (8B) • F245 (9C-11C, 11D)
	DMA subchannel x and x error	• DMARDY PAL (13C) • 82258 (8B) • F245 (9C-11C, 11D)
	DMA channel 2 transmit error (External Sync via DREQ signal) Expected Data = 21h, Received Data = xxxxh	• DMARDY PAL (13C) • 82258 (8B) • F245 (9C-11C, 11D)
(47) MDC WorkNet Loopback	WorkNet loopback test failed (data transfer rate is .75 Mbits/s)	• SCC (17B) • Network free ckts. • 75174 (12A) • 75175 (13A)
	WorkNet loopback test failed (data transfer rate is 1.4 Mbits/s)	• SCC (17B) • Network free ckts. • 75174 (12A) • 75175 (13A)
	WorkNet loopback test failed (SDLC mode)	• SCC (17B) • Network free ckts. • 75174 (12A) • 75175 (13A)
	DTR timeout error	• SCC (17B) • Network free ckts. • 75174 (12A) • 75175 (13A)

Table 4-5. Multidrop Communications FDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
(47) MDC WorkNet Loopback (Cont.)	**Transmit timeout error**	• SCC (17B) • Network free ckts. • 75174 (12A) • 75175 (13A)
	Receive character parity error	• SCC (17B) • Network free ckts. • 75174 (12A) • 75175 (13A)
	Receive character overrun error	• SCC (17B) • Network free ckts. • 75174 (12A) • 75175 (13A)
	CRC error **Receive character framing error**	• SCC (17B) • Network free ckts. • 75174 (12A) • 75175 (13A)
(48) MDC Multidrop Loopback	**Compare error = x** **Multidrop loopback test failed (data transfer rate is 1.4 Mbits/s)**	• SCC (16B) • Network free ckts. • 75174 (12A) • 75175 (13A)
	Multidrop loopback test failed (SDLC mode)	• SCC (16B) • Network free ckts. • 75174 (12A) • 75175 (13A)
	DTR timeout error	• SCC (16B) • Network free ckts. • 75174 (12A) • 75175 (13A)

Table 4-5. Multidrop Communications FDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
(48) MDC Multidrop Loopback (Cont.)	Receive character parity error	• SCC (16B) • Network free ckts. • 75174 (12A) • 75175 (13A)
	Receive character overrun error	• SCC (16B) • Network free ckts. • 75174 (12A) • 75175 (13A)
	CRC error Receive character framing error	• SCC (16B) • Network free ckts. • 75174 (12A) • 75175 (13A)
	Compare error = x	• SCC (16B) • Network free ckts. • 75174 (12A) • 75175 (13A)
	Transmit timeout error	• SCC (16B) • Network free ckts. • 75174 (12A) • 75175 (13A)
(49) MDC Timer	MDC Timer Register Write/Read Error CIO Register = xxxxh Expected Data = xxxxh Received Data = xxxxh	• 8536 (15B) • 82258 (8B)
	MDC Timer x Count Down Error	• 8536 (15B) • 82258 (8B)
	MDC Timer x Interrupt Failed	• 8536 (15B) • 82258 (8B)

Table 4-5. Multidrop Communications FDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
(50) MDC Baud Rate	**Baud rate test failed, time constant = xxxxh**	• SCC (16B)
	Baud rate test failed, transmit timeout error	• SCC (16B)
(51) MDC External Loopback	**DTR/DSR handshake not responding**	• SCC (16B) • Network free ckts. • 75174 (12A) • 75175 (13A)
	Handshake signal change unexpectedly	• SCC (16B) • Network free ckts. • 75174 (12A) • 75175 (13A)
	Receive Character Timeout at the First Character	• SCC (16B) • Network free ckts. • 75174 (12A) • 75175 (13A)
	Receive Character Timeout at the Second Character	• SCC (16B) • Network free ckts. • 75174 (12A) • 75175 (13A)
	Receive Character Timeout at the Third Character	• SCC (16B) • Network free ckts. • 75174 (12A) • 75175 (13A)
	Receive Character Timeout at the xth Character	• SCC (16B) • Network free ckts. • 75174 (12A) • 75175 (13A)

Table 4-5. Multidrop Communications FDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
(51) MDC External Loopback (Cont.)	**Port x Sync Signals Test Failed**	• SCC (16B) • Network free ckts. • 75174 (12A) • 75175 (13A)
	RTS/CTS handshake not responding	• SCC (16B) • Network free ckts. • 75174 (12A) • 75175 (13A)
	Expected data = xxxxh, Received data = xxxxh	• SCC (16B) • Network free ckts. • 75174 (12A) • 75175 (13A)
	Compare Error = x	• SCC (16B) • Network free ckts. • 75174 (12A) • 75175 (13A)
	Transmit data = xxxxh, Receive data = xxxxh	• SCC (16B) • Network free ckts. • 75174 (12A) • 75175 (13A)
(52) MDC Internal Loopback	**Receive Character Timeout at the First Character**	• SCC (16B) • Network free ckts. • 75174 (12A) • 75175 (13A)
	Receive Character Timeout at the Second Character	• SCC (16B) • Network free ckts. • 75174 (12A) • 75175 (13A)

Table 4-5. Multidrop Communications FDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
(52) MDC Internal Loopback (Cont.)	Transmit data = xxxxh, Receive data = xxxxh	• SCC (16B) • Network free ckts. • 75174 (12A) • 75175 (13A)
	Receive Character Timeout at the Third Character	• SCC (16B) • Network free ckts. • 75174 (12A) • 75175 (13A)
	Receive Character Timeout at the xth Character	• SCC (16B) • Network free ckts. • 75174 (12A) • 75175 (13A)
	Compare Error = x	• SCC (16B) • Network free ckts. • 75174 (12A) • 75175 (13A)
(55) TCU -8 External Loopback	No response from TCU-8 address from x1 to x2	• TCU-8 • Network cables
	TCU-8 channel x (address y) RTS/CTS handshake not responding	• TCU-8 • Network cables
	TCU-8 channel x (address y) compare error	• TCU-8 • Network cables

Chapter 5
Monitor Debugger

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INTRODUCTION

The system firmware consists of the system (or resident) monitor program which is a collection of routines that remain permanently in programmable read-only memory (PROM) on the CPU board. The function of the monitor program is to validate the system and provide down-load and disk-boot capability which permits the user to load operating systems and programs into the system memory.

The monitor program consists of three routines: power-up, disk-boot, and debugger. The debugger routine is a development tool included in the monitor for hardware debugging as well as software program development. The debugger allows the user to single step a program or control execution by means of a breakpoint and also allows the user to examine/change particular registers, ports, and memory locations.

A breakpoint allows the user to control execution by placing a software interrupt in the object code at locations specified by the user. The breakpoint transfers control to the debugger and allows the user to replace the original object code at any location and to view the current status.

The system contains a minimum of five printed circuit boards. Three of these boards have microprocessors: the central processing unit (CPU), file processor, and communications (multidrop and/or SIO) boards. Each of the three microprocessor-based boards performs dedicated functions with the main processing tasks executed by the CPU board.

The terminal and network communications are performed by the communications board(s) while the file processor board handles the storage device support. Each of these boards has its own firmware support, which provides power-up verification, hardware initialization, and user monitor call support in a local environment. In addition, the communications board firmware coordinates the system-level power-up sequences as well as monitoring the overall communication between all the firmware at power-up time.

This chapter describes the communication protocol and debugger information for the CPU, file processor, and both the multidrop and SIO communications boards.

MONITOR COMMUNICATION PROTOCOL

Monitor communication between the CPU, communications, and file processor firmware is accomplished through groups of parameter blocks in the system memory. All communication requires CPU intervention except during power-up. Thus, no direct communication between controllers is allowed.

For example, if the file processor needs to print a message, it must send the print command to the CPU board, which will then route the request to the communications board for actual display.

During power-up time, the primary communications board firmware assigns each controller (e.g., file processor, up to three other communications boards, and the CPU board) a 320 byte space in system memory (64 bytes for the parameter block and 256 bytes for the buffer) to be used as the parameter block and message buffer. Subsequently, all communications are done on a one-to-one basis between the CPU and file processor, or between the CPU and the individual communications boards.

CPU Debugger Commands

The CPU debugger commands are interactive and are categorized into those commands that require parameter(s) and those that do not. Most commands are invoked by entering one to two characters (ID). To execute the first category of commands (those that require parameters), all you do is enter the command ID, followed by a Space Bar. Then a prompt automatically asks you to input the parameters, one at a time. The Space Bar is used to terminate or to skip inputing the current data field and advance to the next data field. The default value will be assumed for any skipped parameters.

Pressing the Retn key will terminate the data input and cause the command to be executed. To execute the second category of commands (those that do not require parameters), you are required to enter the command character(s) followed by a Retn.

Debugger Command Conventions

The following conventions are used in the debugger command descriptions:

- underscore (_) denotes a space in the command lines
- unless otherwise indicated, all values are specified in hexadecimal form
- upper or lower case letters are accepted
- all memory addresses are six hexadecimal digits long
- all I/O addresses are four hexadecimal digits long
- symbol ^ denotes a control key

NOTE

Currently, some messages displayed on the console screen during diagnostic testing may show the carriage return as <CR>. However, on most terminal keyboards the Retn key is the carriage return function. In all cases Retn is used here to indicate the carriage return function.

The CPU debugger commands are:

A	Alter Memory
B	Display Breakpoints
BC	Clear All Breakpoints
BC*n*	Clear Breakpoint *n*
BS*N*	Set Breakpoint *n*
C	Display Register
C0	Change 8 Bit Registers
C1	Change 16 Bit Registers
C2	Change 32 Bit Registers
CS	Change Segment Registers
D	Display Memory Contents
E	Execute
EA	Execute Address

FB	Fill Memory Byte
FW	Fill Memory Word
FD	Fill Memory Double Word
H	Switch to SIO Monitor
Z	Switch to Multidrop Monitor
J	Rewind Tape
L	Remote Download
M	Move Memory
I	Input CPU Local Port
IF	Input File Processor Local Port
O	Output CPU Local Port
OF	Output File Processor Local Port
OS	Output System Port
RF	Read Floppy Low Speed
RFH	Read Floppy High Speed
RH	Read Hard Disk
RT	Read Tape
WF	Write Floppy Low Speed
WFH	Write Floppy High Speed
WH	Write Hard Disk
WT	Write Tape
WP	Write Printer
S	Single Step
T	Display Time
TS	Set Time
U	Upload Into System Memory
X	Multiprocessor Test
?	Display Help Screen
??	Help

The CPU debugger commands are executed as follows:

Alter Memory (A Space Bar)

This command allows you to change the memory contents, one byte at a time, beginning with the given address. The contents of the consecutive memory locations can be altered by entering the Space Bar repeatedly. This command is terminated by entering the Retn. The parameters are:

Address = physical address (hex)
Contents = byte(hex)

Display Breakpoints (B Retn)

This command displays which 80386 internal breakpoint registers have been set.

Clear All Breakpoints (BC Retn)

This command disables all the breakpoints.

Clear Breakpoint *n* (BC*n* Retn)

This command allows you to disable one of the four 80386 breakpoint registers. Where *n* = 0, 1, 2, and 3.

Set Breakpoint *n* (BS*n* Space Bar)

This command allows you to set up one of the four 80386 breakpoint registers. Where *n* = 0, 1, 2, and 3. The parameters are:

Address = physical address
Condition = the control option for the specified breakpoint

There are seven control options, the following inputs are allowed:

e, e1, w1, w2, w4, b1, b2, b4. Where:
e = instruction execution only
w = data write only
b = data read or data write
1/2/4 specifies the length of breakpoint field

Display Register (C Retn)

This command allows you to look at the contents of the 80386 internal registers.

Change 8 Bit Registers (C0 Space Bar)

This command allows you to change all the 8 bit registers. The parameters are:

Name = al, ah, bl, bh, cl, ch, dl, dh
Contents = byte(hex)

Change 16 Bit Registers (C1 Space Bar)

This command allows you to change all the 16 bit registers. The parameters are:

Name = ax, bx, cx, dx, si, di, bp, sp, ip
Contents = word(hex)

Change 32 Bit Registers (C2 Space Bar)

This command allows you to change all the 32 bit registers. The parameters are:

Name = eax, ebx, ecx, edx, esi, edi, ebp, esp, eip
Contents = double word(hex)

Change Segment Registers (CS Space Bar)

This command allows you to change the contents of the segment registers. The parameters are:

Name = cs, ds, es, fs, gs, ss
Contents = word(hex)

Display Memory Contents (D Space Bar)

This command allows you to display the contents of consecutive memory locations starting with a given address, one full screen at a time. If the displayed locations are more than one full screen can hold, you can type Retn to exit or any other keys (except some special keys) to display the rest of the locations. The parameters are:

Length = word(hex), specifying number of bytes

If the length is zero, 65536 bytes will be assumed.

Execute (E Retn)

This command allows you to run the program starting at the current cs:eip.

Execute Address (EA Space Bar)

This command allows you to run the program starting at a given physical address. The parameter is:

Address = physical address

Fill Memory Byte (FB Space Bar)

This command allows you to fill memory byte-locations starting at the given address with given data pattern. The parameters are:

Address = physical address
Length = word(hex), specifying number of bytes

If the length is zero, 65536 bytes will be assumed.

Contents = byte(hex)
Pattern = data pattern type: f(fix), i(increment), d(decrement)

Fill Memory Word (FW Space Bar)

This command allows you to fill memory word-locations starting at the given address with given data pattern. The parameters are:

Address = physical address
Length = word(hex), specifying number of words

If the length is zero, 65536 words will be assumed.

Contents = word(hex)
Pattern = data pattern type: f(fix), i(increment), d(decrement)

Fill Memory Double Word (FD Space Bar)

This command allows you to fill memory double word-locations starting at the given address with given data pattern. The parameters are:

Address = physical address
Length = word(hex), specifying number of double words

If the length is zero, 65536 double words will be assumed.

Contents = word(hex)
Pattern = data pattern type: f(fix), i(increment), d(decrement)

Switch TO SIO/Multidrop Monitor (H Retn or Z Retn)

This command allows you to switch to SIO/Multidrop monitor.

Rewind Tape (J Retn)

This command allows you to rewind the tape.

Remote Download (L Retn)

This command is for remote downloading.

Move Memory (M Space Bar)

This command allows you to relocate a block of memory data to desired location. The parameters are:

Source Address = phsical address to be moved from
Destination Address = phsical address to be moved to
Length = word(hex), specifying number of bytes

If the length is zero, 65536 bytes will be assumed.

Input CPU Local Port (I Space Bar)

This command allows you to read in the word value of the CPU local port destinated in the given address. The parameter is:

Port Address = word(hex), specifying the offset address of the local port

Input File Processor Local Port (IF Space Bar)

This command allows you to read in the word value of the file processor local port destinated in the given address. The parameter is:

Port Address = word(hex), specifying the physical address of the local port

Output CPU Local Port (O Space Bar)

This command allows you to write a word value to the CPU local port destinated in the given address. The parameters are:

Port Address = word(hex), specifying the offset address of the local port
Contents = word(hex)

Output File Processor Local Port (OF Space Bar)

This command allows you to write a word value to the file processor local port destinated in the given address. The parameters are:

Port Address = word(hex), specifying the physical address of the local port
Contents = word(hex)

Output System Port (OS Space Bar)

This command allows you to write a word value to the system port destinated in the given address. The parameters are:

Port Address = word(hex), specifying the offset address of the system port
Contents = word(hex)

Read Floppy Low Speed (RF Space Bar)

This command allows you to read from the low speed floppy disk. The parameters are:

Buffer Address = physical address
Cylinder number = 0 to 4Fh
Head = 0, 1
Start Sector = 0 to 8
Sector Count = 1 to 9

Read Floppy High Speed (RFH Space Bar)

This command allows you to read from the high speed floppy disk. The parameters are:

Buffer Address = physical address
Cylinder number = 0 to 4Fh
Head = 0, 1
Start Sector = 0 to 0Eh
Sector Count = 1 to 0Fh

Read Hard Disk (RH Space Bar)

This command allows you to read from the high speed floppy disk. The parameters are:

Buffer Address = physical address
Cylinder number = 0 to 3FFh
Drive Number = 0 to 2
Head = 0 to 0Fh
Start Sector = 0 to 22h
Sector Count = 1 to 23h

Read Tape (RT Space Bar)

This command allows you to read from the tape. The parameters are:

Buffer Address = physical address
Number of blocks = 1 to 79h

Write Floppy Low Speed (WF Space Bar)

This command allows you to write to the low speed floppy disk. The parameters are:

Buffer Address = physical address
Cylinder number = 0 to 4Fh
Head = 0, 1
Start Sector = 0 to 8
Sector Count = 1 to 9

Write Floppy High Speed (WFH Space Bar)

This command allows you to read from the high speed floppy disk. The parameters are:

Buffer Address = physical address
Cylinder number = 0 to 4Fh
Head = 0, 1
Start Sector = 0 to 0Eh
Sector Count = 1 to 0Fh

Write Hard Disk (WH Space Bar)

This command allows you to write to the high speed floppy disk. The parameters are:

Buffer Address = physical address
Cylinder number = 0 to 3FFh
Drive Number = 0 to 2
Head = 0 to 0Fh
Start Sector = 0 to 22h
Sector Count = 1 to 23h

Write Tape (WT Space Bar)

This command allows you to write to the tape. The parameters are:

Buffer Address = physical address
Number of blocks = 1 to 79h

Write Printer (WP Space Bar)

This command allows you to send characters resided on the memory to the printer. The parameters are:

Buffer Address = physical address
Number Of Bytes = word value(hex)

Single Step (S Retn)

This command allows you to execute a single instruction at current cs:eip.

Display Time (T Retn)

This command displays the time of the real time clock chip.

Set Time (TS Space Bar)

This command allows you to set the time of the real time clock chip. The parameters are:

Second = 0 to 59h
Minute = 0 to 59h
Hour = 0 to 23h
Day of Week = 1 to 7, 1=SUN, 7=SAT
Month = 1 to 12h
Date = 1 to 31h
Year = 1986 to 2100h

Upload Into System Memory (U Retn)

This command allows the SIO/multidrop to upload the code into system memory from the console port and transfers control to the loaded code.

Multiprocessor Test (X Retn)

This command allows you to test the ability of multiple CPUs accessing the system bus concurrently (not supported at this printing).

Display Help Screen (? Retn)

This command displays all the debugger commands.

Help (?? Space Bar)

This command gives you more information about a specific command. The parameter is:

Command Identifier = command ID

Special Control Keys

The following keys provide some special control functions:

!	repeats the last executed command
Ctrl-d	causes the next executed command to loop forever
Ctrl-c	aborts the command executed in a loop
Ctrl-r	restarts monitor operation and prints boot menu
Ctrl-v	displays the internal version number of monitor
Ctrl-w	switches to cpu-a monitor
Ctrl-x	switches to cpu-b monitor
Ctrl-y	switches to cpu-c monitor
BS	removes the last character/prompt
Del	erases the current input line

Space Bar has the following data input control functions:

- prompts the first data field of the last executed command if it is entered as the first character of command
- prints the current data field of the last executed command if it is entered as the first character of data field
- goes on to the next data field of the command if it is entered as the last character of data field

Communications Debugger Commands (Software Mode)

The multidrop/SIO communications debugger commands (software mode) are:

A	Alter Memory
B	Set Baud rate
C	Set Registers
D	Display Memory
F	Fill Memory
G	Go and Execute User Code
H	Remote Download
I	Input From Port
L	Remote Download to CPU
O	Output to Port
R	Hex Download
S	Single Step
U	Users Console Into Memory Buffer
W	Send the W Character to Ports 0 and 1 (FCC RF Test)
X	Execute Users Memory Buffer
Z	Go to Main CPU Monitor
?	Display Command Menu
Break	Switch to hardware mode

The communications debugger commands (software mode) are executed as follows:

A Alter Memory

Syntax:

A <*address*> <*data*> <*data*> <*data*>...<*data*> Retn

Alter local memory. Enter data in hexadecimal. No delimiter is needed between the command character and the address. All other parameters need a delimiter.

C Set Registers

Syntax:

Cxx <*data*> Retn

Set or display the users CPU registers. At power-up these are all set to the 0 default value. A hexa decimal down-load will set the CS:IP if there is a start record. The following is a list of the registers:

CS, IP, AX, BX, CX, DX, FL, SS, SP, BP, DS, SI, ES, and DI.

To display all the registers just type **C** Retn. To change a register, type **C** followed by the register name from above, a space character, then the hexadecimal data, and finally a cursor return. Enter data in hexadecimal. No delimiter is needed between the command character and the register name. The data needs a delimiter.

D Display Memory

Syntax:

D<*address*> <*length*> Retn

Display local or system memory. Length can be any hexadecimal number from 0 to FFFF, where 0 = 65536. A Ctrl-d will repeat the command until a Ctrl-c. System memory can be displayed from the window at 80000 to BFFFF. The window page register can be changed by outputing to the SYSPAGE port.

No delimiter is needed between the command character and the address. The length needs a delimiter.

F Fill Memory

Syntax:

F<*address*> <*length*> <*data*> Retn

Fill local or system memory. Same as hardware mode.

G Go and Execute User Code

Syntax:

G Retn

Go from the CS:IP setup in the users registers.

NOTE

You can set as many breakpoints as you like by replacing the op code with the CC instruction.

H Remote Download

Used for remote diagnostics.

I Input From Port

Syntax:

I<*port*> Retn

Input from local or system port. A Ctrl-i will input continuously until stopped by a Ctrl-c. No delimiter is needed between the command character and the port address.

L Remote Download to CPU

Proprietary format. Used for remote diagnostics.

O Output to Port

Syntax:

O<*port*> <*data*> <*data*>... <*data*> Retn

Output to local or system port. A Ctrl-o will output continuously until stopped by a Ctrl-c.

No delimiter is needed between the command character and the port address. The data needs delimiters.

R Hex Download

Syntax:

H<*TTYport*> Retn

Hexadecimal file down-load. Uses Intel hexadecimal file format. The TTY port can be any number from 0 to 4, where 0 is the console.

S Single Step

Syntax:

S Retn

Single step one instruction. The CS:IP must already be pointing to some valid users code. Instructions that move to/from the segment registers may cause the next instruction to be executed automatically. There is nothing the monitor can do about this and it is not a bug.

U Users Console Into Memory Buffer

Syntax:

U<*address*> Retn

W Send the W Character to Ports 0 and 1.

Syntax:

W Retn

This is an FCC test to check for proper RF noise levels. This is not a debug command. To stop this test type Ctrl-c.

X Execute Users Memory Buffer

Syntax:

X<*address*> Retn

Z Go to Main CPU Monitor

If the main CPU is running, this command will appear in the menu. If there are problems with the main CPU, then this command will not appear in the menu. If this command is functioning, control will pass to the CPU.

Multidrop Communications Debugger Commands (Hardware Mode)

The multidrop communications debugger commands (hardware mode) are:

A	Strobe All I/O Chips
B	Set Baud rate
C	Checksum Memory
D	Display Memory
E	Examine ADMA Internal Registers
F	Fill Memory and Verify
G	Go and Execute User Code
H	DMA Scope Loop
I	Input From Port
K	Toggle the "Keep NMI Enabled" Flag
L	Serial Port Loopback Test (requires loopback connectors)
M	Multidrop Test (Multidrop Port)
N	Network Test (WorkNet Port)

O	Output To Port
S	SCC Recovery Exerciser (scope loop)
T	Timer Exerciser
U	Enter User-Defined Macro Into Memory
W	Memory Write Without Verify (Scope Loop)
X	User-Defined Macro
Z	Transfer Control to Main CPU Monitor
?	Display Command Menu
Break	Switch between hardware and software mode
Ctrl-c	Aborts any test and returns to command level
Ctrl-v	Shows monitor program version number

NOTE

Most commands will repeat if entered as a control character. A Ctrl-c will stop the test.

The multidrop communications debugger commands (hardware mode) are executed as follows:

A Strobe All I/O Chips

This command does an INPUT of the base port of all I/O ICs on the local bus and executes continuously until interrupted by Ctrl-c.

B Set Baud Rate

Syntax:

B <*port*> <*baud rate*>

This command sets up the baud rate for any serial port on the multidrop communications board <*port*> ranges from 0 to 5 and <*baud rate*> can be any value from 100 to 38,400 baud.

C Checksum Memory

Syntax:

C <*start.addr*> <*length*>
^C <*start.addr*> <*length*>

This command checksums <*length*> bytes of memory starting at <*start.addr*>. The hexadecimal value of the checksum is displayed on the console. This test executes fast enough to be used as a scope loop.

D Display Memory

Syntax:

D <*start.addr*> <*length*>
^D <*start.addr*> <*length*>

This command displays the contents of <*length*> bytes of memory starting at <*start.addr*>. Both hexadecimal and ASCII values are displayed at 16 bytes per line.

E Examine ADMA Internal Registers

Syntax:

E

This command displays the contents of all registers in the DMA controller.

If the ADMA's multiplexer channels are running, executing this command may cause problems with tests H4-H10 because a read of the LIVR (last interrupt vector register) pops the last interrupt vector off of the ADMA's internal stack.

F Fill Memory

Syntax:

F <*start.addr*> <*length*> <*data*>
^F <*start.addr*> <*length*> <*data*>

This command fills <*length*> bytes of memory beginning at <*start.addr*>, with <*data*>, a byte at a time. Immediately after being written, the byte is read back to insure that it stored properly. If the data read does not compare with the data written, an error message is displayed. <*data*> must be either a byte value or "i". If <*data*> = "i", then an incrementing byte pattern (starting at 0) is used.

If the Ctrl-f version of the command is entered and "i" is specified for <*data*>, the starting value of the incrementing pattern is incremented at each pass.

G Go and Execute User Code

Syntax:

G Retn

Go from the CS:IP setup in the users registers.

NOTE

You can set as many breakpoints as you like by replacing the op code with the CC instruction.

H DMA Scope Loop

Syntax:

```
H <number>      ; Start DMA <number>
HS              ; Stop all DMAs now
H               ; Stop all DMAs slowly
```

These commands set up one or two DMA channels and the associated serial communications controller (SCC) to transfer bytes between the SCC and memory under DMA control. Except for H0, H1, and H2, the SCC is programmed for 9600 baud, asynchronous.

Any H test (except for H9 or H10) can be run in the background with other tests, if desired. Upon terminal count, an interrupt to the input/output processor (IOP) is generated, and the channel is reprogrammed to repeat the process.

Tests H9 and H10 run only one pass. The other tests run until stopped with the H or HS command. Table 5-1 is a summary and a detailed description of the H commands:

Table 5-1. H Command Descriptions

Command	ADMA Ch.	Function	Tx From	Rx To	Port	Connector	SCC
H0	0	Tx	0-64K	N/A	4	P14	SCC2-B
H1	1	Tx	1000h	N/A	Mltidrp	J15	SCC3-B
H2	2	Loopback	1000h	2000h	4	P14	SCC2-B
H3	3.6	Tx	1000h	N/A	3	P13	SCC1-A
H4	3.6,3.7	Loopback	1000h	4000h	3	P13	SCC1-A
H5	3.4	Tx	1000h	N/A	2	P12	SCC1-B
H6	3.4,3.5	Loopback	1000h	6000h	2	P12	SCC1-B
H7	3.2	Tx	1000h	N/A	1	P11	SCC0-A
H8	3.2,3.3	Loopback	1000h	8000h	1	P11	SCC0-A
H9	3.0	Tx	1000h	N/A	0	P10	SCC0-B
H10	3.0,3.1	Loopback	1000h	A000h	0	P10	SCC0-B

HS - Stops all H tests immediately.

H - Stops each H test upon terminal count.

H0 - This command uses ADMA channel 0 and SCC2-B to transmit the contents of local RAM from 0-64K out to port 4 (P14) at 1.4M baud, asynchronous.

H1 - This command uses ADMA channel 1 and SCC3-B (at 1M baud, synchronous) to transmit a 4K block of local RAM (an incrementing pattern starting at address 1000h) to the multidrop port (J15).

H2 - This command uses ADMA channels 0 and 2 and SCC2-B (port 4, P14) at 1.4M baud, asynchronous, in a full-duplex internal loopback configuration. ADMA channel 0 causes the SCC to transmit 4K bytes of data from local RAM (an incrementing pattern starting at address 1000h), which the SCC internally loops back into its own receiver.

ADMA channel 2 is programmed to take the received bytes and place them in local memory starting at address 2000h. Upon channel 2's terminal count, an interrupt is generated which causes the IOP to check the Rx buffer at 2000h for correct data. A pass/fail message is displayed on the console. The ADMA is then reprogrammed to repeat the process.

H3 - This command uses ADMA channel 3 (the multiplexer channel), subchannel 6, and SCC1-A to transmit a 4K block from local RAM (an incrementing pattern starting at address 1000h) to port 3 (P13). Upon terminal count, the test repeats.

H4 - This command uses ADMA channel 3 (the multiplexer channel), subchannels 6 and 7, and SCC1-A (port 3, P13) in a full-duplex internal loopback configuration. ADMA subchannel 6 causes the SCC to transmit 4K bytes of data from local RAM (an incrementing pattern starting at address 1000h), which the SCC internally loops back into its' own receiver.

ADMA subchannel 7 is programmed to take the received bytes and place them in local memory starting at address 4000h. Upon subchannel 7's terminal count, an interrupt is generated which causes the IOP to check the Rx buffer at 4000h for correct data. A pass/fail message is displayed on the console. The ADMA is then reprogrammed to repeat the process.

H5 - This command uses ADMA channel 3 (the multiplexer channel), subchannel 4, and SCC1-B to transmit a 4K block from local RAM (an incrementing pattern starting at address 1000h) to port 2 (P12). Upon terminal count, the test repeats.

H6 - This command uses ADMA channel 3 (the multiplexer channel), subchannels 4 and 5, and SCC1-B (port 2, P12) in a full-duplex internal loopback configuration. ADMA subchannel 4 causes the SCC

to transmit 4K bytes of data from local RAM (an incrementing pattern starting at address 1000h), which the SCC internally loops back into its' own receiver. ADMA subchannel 5 is programmed to take the received bytes and place them in local memory starting at address 6000h.

Upon subchannel 5's terminal count, an interrupt is generated which causes the IOP to check the Rx buffer at 6000h for correct data. A pass/fail message is displayed. The ADMA is then reprogrammed to repeat the process.

H7 - This command uses ADMA channel 3 (the multiplexer channel), subchannel 2, and SCC0-A to transmit a 4K block from local RAM (an incrementing pattern starting at address 1000h) to port 1 (P11). Upon terminal count, the test repeats.

H8 - This command uses ADMA channel 3 (the multiplexer channel), subchannels 2 and 3, and SCC0-A (port 1, P11) in a full-duplex internal loopback configuration. ADMA subchannel 2 causes the SCC to transmit 4K bytes of data from local RAM (an incrementing pattern starting at address 1000h), which the SCC internally loops back into its' own receiver. ADMA subchannel 3 is programmed to take the received bytes and place them in local memory starting at address 8000h.

Upon subchannel 3's terminal count, an interrupt is generated which causes the IOP to check the Rx buffer at 8000h for correct data. A pass/fail message is displayed on the console. The ADMA is then reprogrammed to repeat the process.

H9 - This command uses ADMA channel 3 (the multiplexer channel), subchannel 0, and SCC0-B to transmit a 4K block from local RAM (an incrementing pattern starting at address 1000h) to port 0 (P10). This test stops after one pass.

H10 - This command uses ADMA channel 3 (the multiplexer channel), subchannels 0 and 1, and SCC0-B (port 0, P10) in a full-duplex internal loopback configuration. ADMA subchannel 0 causes the SCC to transmit 4K bytes of data from local RAM (an incrementing pattern starting at address 1000h), which the SCC internally loops back into its' own receiver. ADMA subchannel 1 is programmed to take the received bytes and place them in local memory starting at address A000h.

Upon subchannel 1's terminal count, an interrupt is generated which causes the IOP to check the Rx buffer at A000h for correct data. A pass/fail message is displayed on the console. This test stops after one pass.

I Input from I/O port

Syntax:

I <*port.number*>
^I <*port.number*>

This command inputs a byte from <*port.no*> and displays it on the console. If the <*port.number*> is less than 8000h, input is done from the system bus, and an entire word is read and displayed.

CAUTION

Executing this test may cause problems if input is done from the console's port! Other unpredictable results may occur by reading ports which have interrupts enabled (i.e., invalid interrupts may be generated).

K Keep NMI Enabled

Syntax:

K

This command can be used to re-enable the nonmaskable interrupt (NMI) after an earlier NMI has been detected. Normally NMI does not get automatically re-enabled (to prevent excessive NMI messages). Each time K is entered, the K flag is toggled.

L Loopback Test

Syntax:

L <*port.number*>
^L <*port.number*>

This test requires an external loopback connector (wired TxD to RxD, DTR to DSR, and CTS to RTS) to function properly.

This command sequentially toggles both handshake output lines, and tests for a corresponding response on the input handshake lines. If the handshaking is correct, a 256-byte barber-pole pattern is transmitted (at 9600 baud), and compared to the data received.

<*port.number*> can be in the range of 0 through 5.

M Multidrop Port Test

Syntax:

```
MT <data>          ; Multidrop Transmit
MR                 ; Multidrop Receive
M?                 ; Query Multidrop Status
M                  ; Stop Multidrop Test
```

These commands are used to exercise the multidrop port (J15, SCC3-B) and associated DMA channel (ADMA channel 1) in an SDLC mode, at 1M baud. This test is completely interrupt-driven, and runs in the background. Once MT or MR is started, there is no further indication that the test is running.

The following is a detailed description of the M commands:

MT <*data*> - This command sets up ADMA channel 1 and SCC3-B to transmit 1K byte SDLC packets of data to another multidrop communications board (or the network port of the same board).

After the SDLC packet is transmitted, the SCC and DMA channel is reprogrammed to receive a 1K byte packet (buffered at 5800h) which should be echoed by the second communications board (started with MR).

The receive buffer is compared to the transmit buffer, and errors are logged. Data compare, Tx underrun, and short block errors are reported when the test is stopped (by M) or queried (by M?).

The transmit packet is built starting at 5100h in local memory, and contains <*data*>. <*data*> may be either a byte or word value. Specifying "i" for <*data*> produces a binary incrementing pattern.

A word value of DB6C is recommended, since this is a worst-case data pattern. If <*data*> is not specified, whatever data is in the buffer at 5100h is used.

MR - This command sets up ADMA channel 1 and SCC3-B to receive a 1K byte SDLC-formatted packet (buffered at 5100h) from another communications board. Once the packet is received, it is retransmitted back to the sender. The only error checking that is performed is for Tx underruns and short Rx blocks. These errors are logged, and will be displayed by M? or when the test is stopped by M. This test is fully interrupt-driven, and runs in the background which allows other tests to be run simultaneously. Once started, there is no continuous indication of the test status. Use the M? command to report current status.

M? - This command is used to display the error counters for either MT or MR.

M - Entering this command stops MT or MR immediately, and displays the error counters.

N Network (WorkNet) Port Test

Syntax:

```
NT <data>        ; Network Transmit
NR               ; Network Receive
N?               ; Query Network error counters
N                ; Stop Network Test
```

These commands are used to exercise the WorkNet port (P14, SCC2-B) and associated DMA channel (ADMA channel 0) in an SDLC mode, at 1.4M baud. This test is completely interrupt-driven, and runs in the background. Once NT or NR is started, the test continuously displays a running total of the packet count. The following is a detailed description of the N commands:

NT <*data*> - This command sets up ADMA channel 0 and SCC2-B to transmit 1K byte SDLC packets of data to another multidrop communications board (or the multidrop port of this board).

After the SDLC packet is transmitted, the SCC and DMA channel is reprogrammed to receive a 1K byte packet (buffered at 3800h) which

should be echoed by the second communications board (started with NR). The receive buffer is compared to the transmit buffer, and errors are logged. Data compare, Tx underrun, and short block errors are reported when the test is stopped (by N) or queried (by N?).

The transmit packet is first built starting at 3100h in local memory, and contains <*data*>. <*data*> may be either a byte or word value. If "i" is specified for <*data*>, a binary incrementing pattern is used. A word value of DB6C is recommended, since this is a worst-case data pattern. If <*data*> is not specified, whatever data is in the buffer at 3100h is used.

NR - This command sets up ADMA channel 0 and SCC2-B to receive a 1K byte SDLC packet (buffered at 3100h) from another communications board. Once the packet is received, it is retransmitted back to the sender.

The only error checking performed is for Tx underruns and short Rx blocks. These errors are logged, and are displayed by N? or when the test is stopped by **N.** This test is fully interrupt-driven, and runs in the background which allows other tests to be run simultaneously. Once started, a packet counter is incremented and displayed for each packet received. Use the N? command to report current status with error counts.

N? - This command is used to display the error counters for either NT or NR.

N - Entering this command stops NT or NR immediately, and displays the error counters.

O Output to I/O Port

Syntax:

O <*port.number*> <*data*> <*data*> <*data*> ... <*data*>
^**O** <*port.number*> <*data*> <*data*> <*data*> ... <*data*>

This command outputs from 1 to 16 bytes of <*data*> to the port specified by <*port.number*>.

CAUTION

A carelessly-done output can cause the console's port to be unusable. It may be necessary to do a hardware reset to correct the problem.

S SCC Recovery Exerciser

Syntax:

S <*port.number*>
^S <*port.number*>

This command does a high-speed group of 3 reads, and then 3 writes, of the specified I/O port. The data is treated as "don't cares" in both cases. This is used primarily as a scope loop.

T Timer Exerciser

Syntax:

T <*timer.number*> <*count.value*>
T

This command loads timer <*timer.number*> (which ranges from 1 to 3) with <*count.value*> (which ranges from 500h to 0FFFFh) and starts the timer. Upon timeout, an interrupt to the IOP is generated, and the timer automatically reloads itself. On the console, the IOP prints a single digit corresponding to <*timer*> each time the timer times out.

Since these tests are fully interrupt-driven, they can be run in the background, along with other tests.

Once started, the timer(s) will continue running until stopped by entering **T**, which stops all timers.

U Enter User-Defined Macro

Syntax:

U <*address*>

After entering **U**, this command accepts the keyboard entry of a string of monitor commands and stores them in local RAM at <*address*> for later execution. Macro entry is terminated with Esc. When in this mode, the monitor prompt changes to . (period) to indicate that commands are not being executed, but are being entered into the user-specified buffer. The macro can be recalled and executed with the X command.

RESTRICTIONS: <*address*> must be within the 1000h to FFFFh range, and each macro must not be longer than 256 bytes (including carriage returns). There is no practical restriction to the number of macros that can be stored, except by the size of local memory.

W Memory Write Exerciser

Syntax:

W <*start.addr*> <*length*> <*data*>
^W <*start.addr*> <*length*> <*data*>

This command performs a high-speed memory write that writes <*data*> to <*length*> bytes of memory, starting at <*start.addr*>.

No data is read back (nor compared) and only bytes are written. This command executes fast enough to be used for a scope loop.

X Execute User-Defined Macro

Syntax:

X <*address*>

This command starts executing the user-defined macro starting at <*address*>, which was previously stored with the U command.

SIO Communications Debugger Commands (Hardware Mode)

The SIO communications debugger commands (hardware mode) are:

A	Strobe All I/O Integrated Circuits
B	Set Baudrate
C	Checksum Memory
D	Display Memory
F	Fill Memory and Verify
H	High-Speed DMA Test
I	Input From Port
L	Serial Port Loopback Test (requires loopback connectors)
N	Network Test
O	Output To Port
S	SCC Recovery Exerciser (scope loop)
T	Timer Exerciser
U	Enter User-Defined Macro
W	Memory Write Without Verify
X	Execute User-Defined Macro
?	Display Command Menu

Break	Switch to software mode
Ctrl-c	aborts any test and returns to command level
Ctrl-s	suspends printout
Ctrl-q	resumes printout

NOTE

Most commands will repeat if entered as a control character. A Ctrl-c will stop the test.

The communications debugger commands (hardware mode) are executed as follows:

A Strobe All I/O Integrated Circuits

This command does a sequential INP, NOP, OUT to the base port of all the I/O integrated circuits (ICs) on the local bus. Then repeats until interrupted by Esc. The NOP ensures that this test does not violate any recovery specifications.

B Set Baud Rate

Syntax:

B<*channel*> <*baud rate*> Retn

This command sets up the baud rate where <*channel*> ranges from 0 to 9 and <*baud rate*> can be any value from 100 to 19,200 baud.

C Checksum Memory

Syntax:

C<*address*> <*length*> Retn

This command checksums memory from <*address*> up to and including <*length*>. The hexadecimal values of each pass of the checksum is displayed across the screen.

D Display Memory

Syntax:

D<*address*> <*length*> Retn

This command displays the contents of memory <*address*> up to and including <*length*>. Both hexa decimal and ASCII values are displayed at 16 bytes per line.

F Fill Memory and Verify

Syntax:

F<*address*> <*length*> <*data*> Retn

This command fills memory from <*address*> through and including <*length*> with <*data*>. The command will write then verify a byte at a time. If <*data*> = I, then an incrementing byte pattern (starting at 0) is used.

H High-Speed DMA Test

Syntax:

H<*channel*> Retn

These commands set up <*channel*> to move bytes to/from the associated SCC IC.

H0 - This command uses DMA channel 0 and SCC0-A to transmit data at 1.4M baud and transmits the contents of RAM from 0 to 64K.

H1 - This command uses DMA channel 1 and SCC0-B to receive data at 9600 baud. The DMA byte count is set to 1000h bytes and received data is placed in memory starting at 1000h.

H2 - This command uses DMA channels 2 and 3, and SCC1-A in a full-duplex interrupt-driven configuration. This test places the SCC in an internal loopback mode which transfers 1000h bytes from memory at location 2000h to the SCC1-A transmitter. Then the 1000h bytes are looped back in the SCC, direct-memory accessed back to memory starting at location 3000h, and compared to verify that the transfer back to memory was accomplished properly.

Once started, this test runs until stopped by entering **H.** (H0, H1, and H2 can all be running simultaneously.) These tests are intended to check hardware timing.

I Input From I/O Port

Syntax:

I<*port*> Retn

This command inputs and displays a byte from <*port*>.

NOTE

Problems may result if input for this test is done from the console port. Unusual results may occur by reading ports that have interrupts enabled.

L Loopback Test

Syntax:

L<*channel*> Retn

This test requires an external loopback connector (wired TxD to RxD, and DTR to DSR) to function properly. <*channel*> can range from 0 through 9. This test outputs a barber-pole pattern on the Tx register, and compares the results from the Rx register. (The baud rate is not preset to any particular value.) The RS-232 DSR output is also wiggled, and the RS-232 DTR line is checked for the proper response.

NT Network Transmit
NR Network Receive

Syntax:

NT<*data*> Retn
NR Retn

NR - This command sets up the DMA controller and SCC0-A to receive a 1K synchronous data link communications (SDLC) packet (buffered at location 3000h) from another communications board. Once the packet is received, it is retransmitted back to the sender and no error checking is performed.

NT <*data*> - This command fills 1K of memory (starting at location 3000h) with <*data*> and sets up the DMA controller and SCC0-A to transmit 1K SDLC packets to another communications board.

After the SDLC packet is transmitted, the SCC0-A and DMA controller are reprogrammed to receive a 1K packet (buffered at location 4000h) returned by the second communications board and compared to the buffer at location 3000h. Errors are logged, but only reported when Ctrl-c stops the test.

<*data*> may be "I" (which creates an incrementing pattern), a byte, or a word value. A word value of DB6C is recommended since this is a worst-case data pattern. If <*data*> is not specified, the buffer at location 3000h is used as-is.

O Output To I/O Port

Syntax:

O<*port*> <*data*> <*data*> <*data*>..... Retn

This command outputs from 1 to 16 bytes of <*data*> to the port specified by <*port*>.

NOTE

A carelessly done output can make the console port unusable. It may be necessary to reset to correct the problem.

S SCC Recovery Exerciser

Syntax:

S<*port*> Retn

This command performs a high-speed group of 3 reads, and then 3 writes of the specified I/O port. The data is treated as don't cares.

T Timer Exerciser

Syntax:

T<*timer*> <*count*> Retn

This command loads the timer <*timer*>, which ranges from 1 to 3, with <*count*> which ranges from 500h to 0FFFFh, and starts the timer.

Upon timeout, an interrupt is generated and the timer is restarted. A single digit corresponding to <*timer*> is printed each time the timer times out. The timer is stopped by entering **T** <*timer*>. A **T** stops all timers. The timers can be run while other tests are running, since the timers are interrupt driven.

U Enter User-Defined Macro

Syntax:

U<*address*> Retn

This command accepts the keyboard entry of a block of monitor commands starting at <*address*> into memory for later execution. Macro entry is terminated with Esc.

When in this mode, the monitor prompt changes to a . (period) to indicate that commands are not being executed, but are being entered into the userspecified buffer. The macro can be recalled and executed with the X command.

RESTRICTIONS: <*address*> must not be within the 0 to 7FFh range. Each macro can be any length up to the maximum number of bytes in memory. All input is redirected into the memory until ESCAPE is typed to return to the command execution mode. The only restriction to the number of macros that can be stored is the size of the memory.

W Memory Write Exerciser

Syntax:

W<*address*> <*length*> <*data*> Retn

This command performs a memory write that writes <*data*> to each memory location specified. No data is read back and only bytes are written.

The Ctrl-w version of this test will perform continuously as a scope loop. A Ctrl-c will stop the test.

X Execute User-Defined Macro

Syntax:

X<*address*> Retn

This command executes the macro at <*address*>, which was previously stored with the U command.

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Chapter 6
Removal/Replacement

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INTRODUCTION

This chapter includes removal and replacement procedures for the field-replaceable units (FRUs). Also provided are instructions for shipping field-replaceable units to an Altos service center for repair or replacement. Refer to **System Description** - Chapter 1 for a description of the field-replaceable units.

NOTE

Altos recommends that the procedures in this chapter be performed by qualified service personnel.

WARNING

Dangerous potentials exist inside the cabinet. Turn off the AC power to the system and unplug the AC power cord before performing the following procedures.

HANDLING STATIC-SENSITIVE DEVICES

Certain precautions must be taken when working with static-sensitive devices, such as, microprocessors, field-effect transistors (FET), complimentary metal-oxide semiconductors, (CMOS), and other large-scale integration (LSI) devices that use metal-oxide semiconductor (MOS) technology. Static charge buildup in a person's body or leakage from an improperly grounded soldering iron can cause static-sensitive device failure.

Before handling a static-sensitive device or a board with such devices attached to it, ground any static voltage that may have accumulated in your body by touching an object that has been earth grounded.

A bare wire wrapped around your wrist and attached to an earth ground is effective when working extensively with static-sensitive devices.

REMOVAL/REPLACEMENT PROCEDURES

The following procedures describe how to remove and replace field-replaceable units. If a field-replaceable unit is to be shipped for repair or replacement, refer to "Shipping a Field-Replaceable Unit" at the back of this chapter.

Removing the Front Panel

Perform the following procedure to remove/replace the front panel (see Figure 6-1):

1. Turn off the Series 2000 power and unplug the AC power cord. (See "Controls, Connectors, and Indicators" in **System Description** - Chapter 1 for the locations of the power switch and power cord connector.)

2. Use a #2 Phillips screwdriver to turn the two fasteners on the bottom of the front panel 1/4-turn counterclockwise.

3. Gently pull the bottom of the front panel just far enough for the panel to clear the bezels on the tape and floppy drives.

CAUTION

Do not pull the bottom of the front panel out too far or you may break the retaining hook at the top of the panel.

4. Push the front panel up to disengage the retaining hook at the top. Then, pull the front panel toward you to free the panel from the cabinet.

5. Replace the front panel by inserting the retaining hook into the slot at the top of the front panel and pivoting the panel down into position.

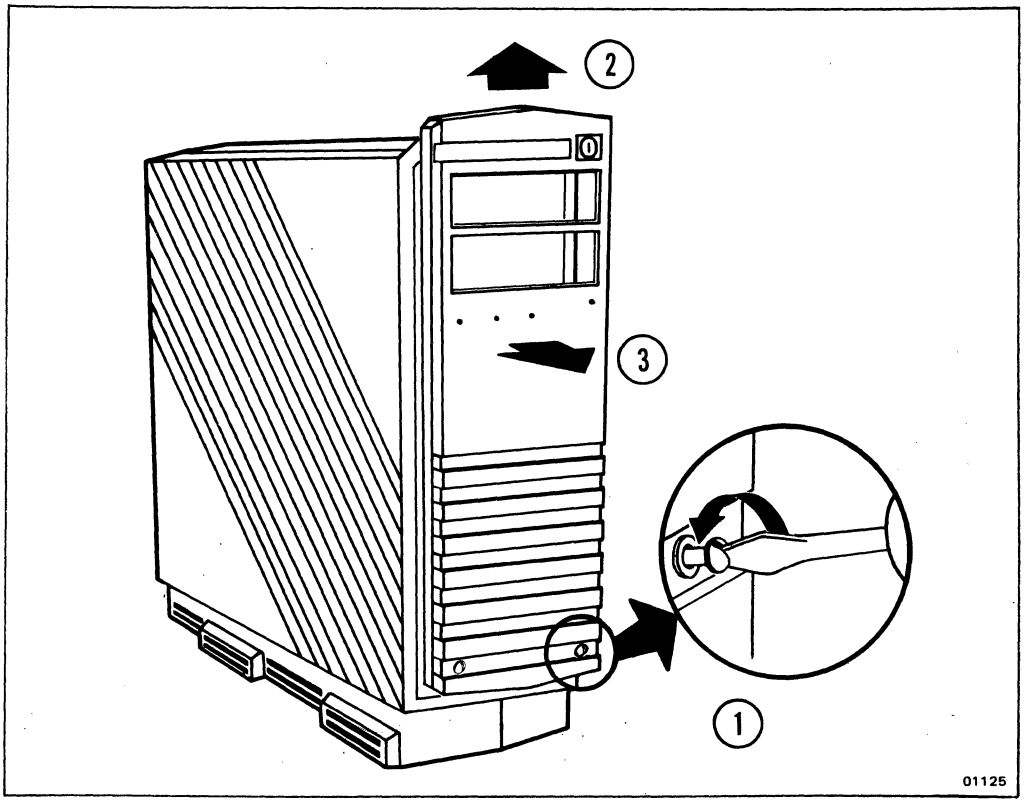


Figure 6-1. Removing/Replacing the Front Panel

Removing the Side Panels

Perform the following procedure to remove/replace the cabinet side panels (see Figure 6-2):

1. Turn off the Series 2000 power and unplug the AC power cord. (See "Controls, Connectors, and Indicators" in **System Description** - Chapter 1 for the locations of the power switch and power cord connector.)

2. Remove the front panel as described previously.

3. Remove the left side panel by using a #2 Phillips screwdriver to remove the two screws on the top and three screws on the bottom. Then remove the screw on the top front of the right side panel.

4. Gently remove the left side panel from the chassis.

5. Remove the right side panel by using a #2 Phillips screwdriver to remove the two screws on the top and three screws on the bottom.

6. Gently remove the right side panel from the chassis.

7. Replace the left side panel by guiding the rear standoff rod through the guide hole bracket near the center of the chassis. Replace and tighten the two screws on the top, three on the bottom, and one on the top front of the right side panel.

NOTE

To make it easier to align the threaded end of the top front standoff rod with the mating screw hole in the right side panel:

a. Remove the tape drive as described previously, but do not disconnect the cables. Gently set the tape drive on top of the computer.

b. Reach up inside the tape drive opening and position the standoff rod so the threaded end is aligned with the hole in the right side panel.

c. Insert the screw into the threaded end of the standoff rod and tighten to secure the side panel.

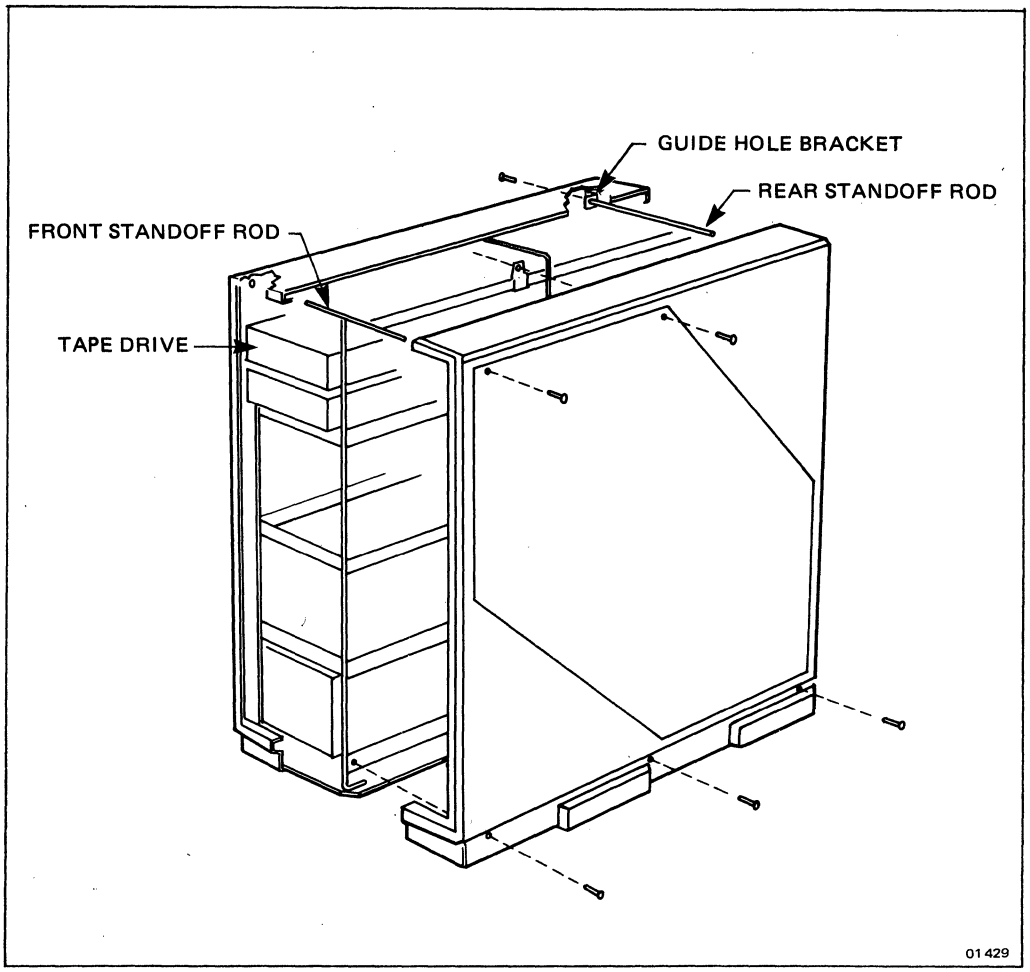


Figure 6-2. Removing/Replacing the Side Panels

Removing the Tape Drive

Perform the following procedure to remove the cartridge-tape drive (see Figures 6-3 and 6-4):

1. Turn off the Series 2000 power and unplug the AC power cord. (See "Controls, Connectors, and Indicators" in **System Description** - Chapter 1 for the locations of the power switch and power cord connector.)

2. Remove the front panel as described previously.

3. Use a #2 Phillips screwdriver to turn the screw on the drive mounting bracket a quarter-turn counterclockwise as shown in Figure 6-3.

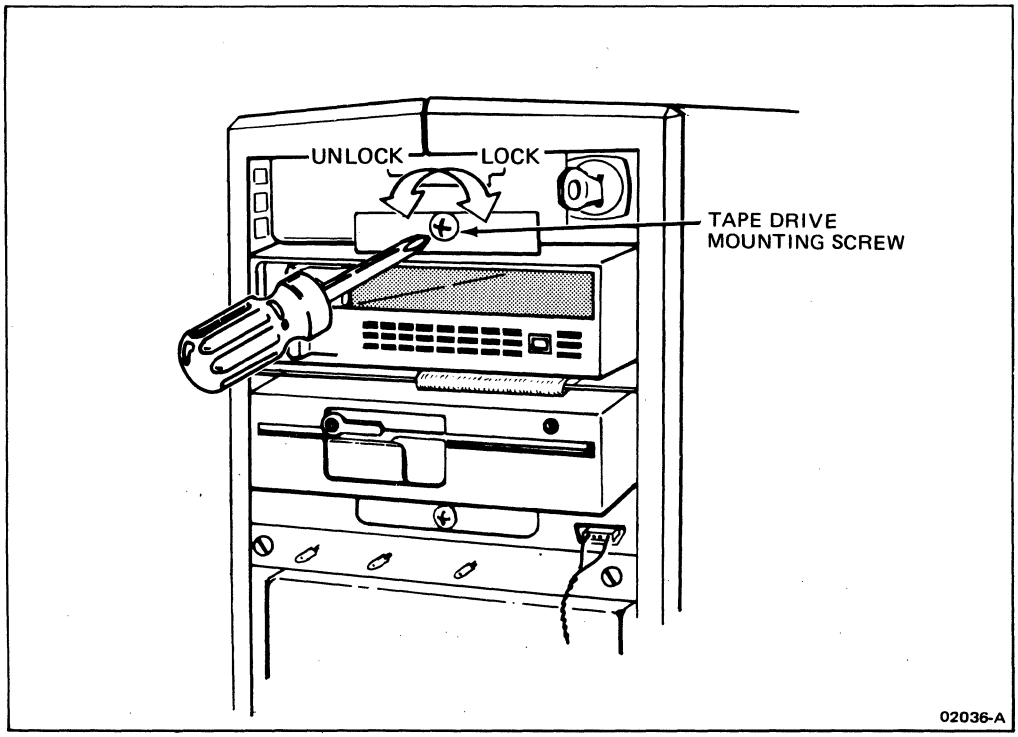


Figure 6-3. Locking/Unlocking the Tape Drive Mounting Screw

4. Slide the tape drive out of the chassis. Notice the two cables connected to the back of the drive and the steel dust cover that protects the cables as shown in Figure 6-4.

5. Remove the dust cover by popping one side out of the grooves.

6. Unplug the two cables and set the drive on a flat surface. **Do not remove the cables from the cabinet.**

7. Replace the tape drive as described in the following procedure.

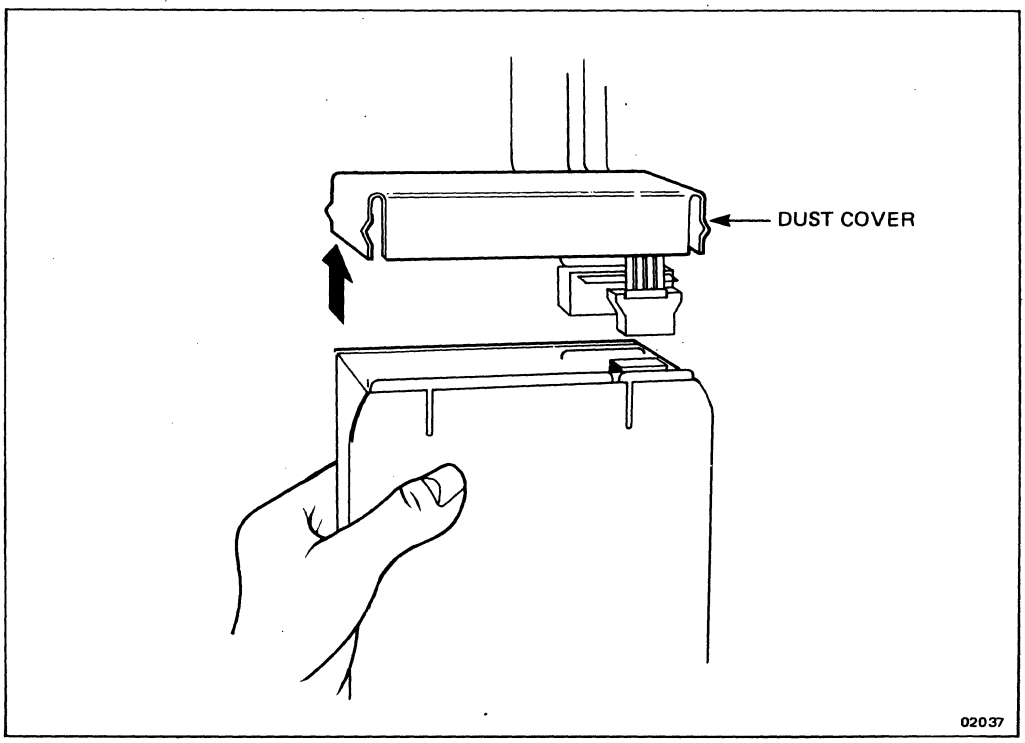


Figure 6-4. Removing/Replacing the Tape Drive

Replacing the Tape Drive

Perform the following procedure to replace the cartridge-tape drive (see Figures 6-3 and 6-4):

1. Turn off the Series 2000 power and unplug the AC power cord. (See "Controls, Connectors, and Indicators" in **System Description** - Chapter 1 for the locations of the power switch and power cord connector.)

2. Position the tape drive with the mounting bracket facing up.

3. Connect the 4-pin power cable connector to the corresponding connector on the back of the drive. (The connector is keyed for the proper orientation.) Be careful not to damage the yellow capacitor on the cable.

4. Connect the 57-pin connector to the corresponding connector on the back of the drive as shown in Figure 6-4. Do not twist the cable -- keep the red cable stripe to your right as you face the back of the system.

5. Install the steel dust cover by placing one end into the grooves at the cable end and pulling the other end over until it pops into place.

6. Slide the drive into the chassis. Guide the cabies back into the chassis as you slide the drive into the slot.

7. Gently press the drive until it seats firmly in the chassis.

8. Use a #2 Phillips screwdriver to press in and turn the locking screw a quarter-turn clockwise as shown in Figure 6-3.

9. Replace the front panel in the reverse order of removal.

Removing the Floppy Drive

Perform the following procedure to remove the floppy disk drive (see Figures 6-5 and 6-6):

1. Turn off the Series 2000 power and unplug the AC power cord. (See "Controls, Connectors, and Indicators" in **System Description** - Chapter 1 for the locations of the power switch and power cord connector.)

2. Remove the front panel as described previously.

3. Use a #2 Phillips screwdriver to turn the screw on the drive mounting bracket a 1/4-turn counterclockwise as shown in Figure 6-5.

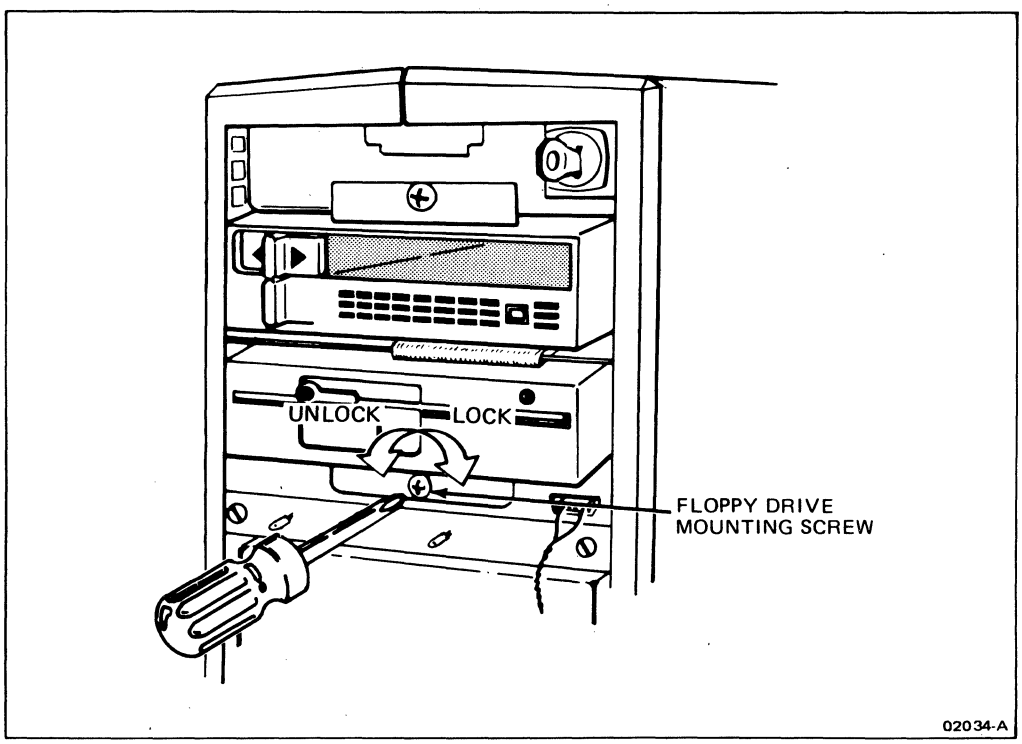


Figure 6-5. Locking/Unlocking the Floppy Drive Mounting Screw

4. Slide the floppy drive out of the chassis. Notice the two cables connected to the back of the drive and the steel dust cover that protects the cables as shown in Figure 6-6.

5. Remove the dust cover by popping one side out of the grooves.

6. Unplug the two cables and set the drive on a flat surface. **Do not remove the cables from the cabinet.**

7. Replace the floppy drive as described in the following procedure.

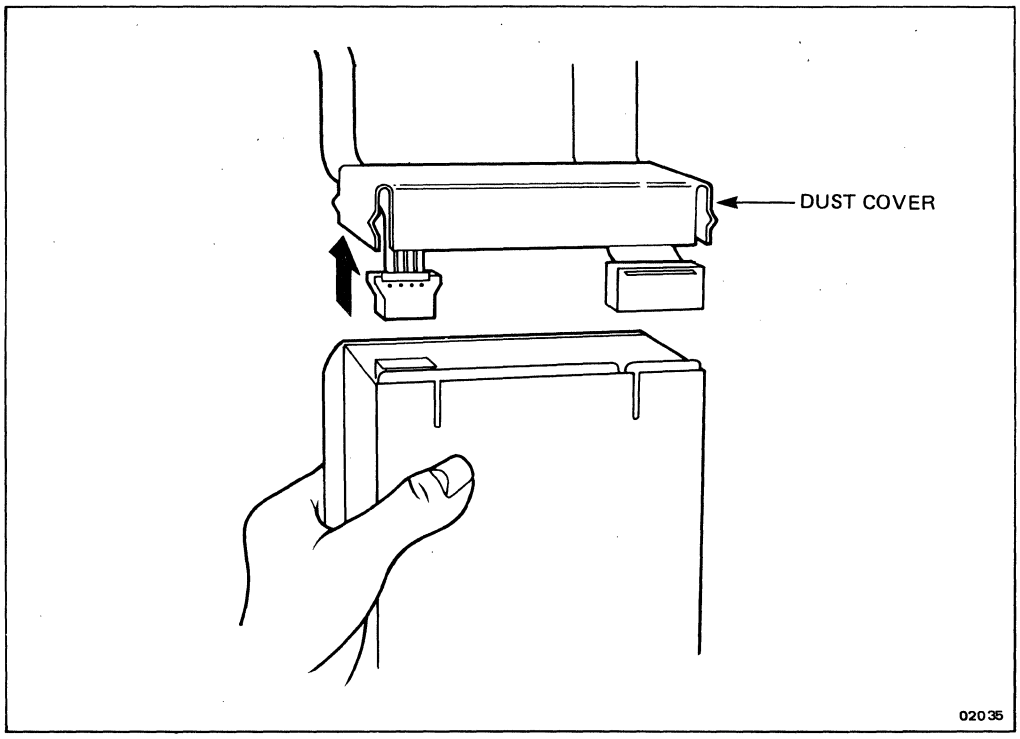


Figure 6-6. Removing/Replacing the Floppy Drive

Replacing the Floppy Drive

Perform the following procedure to replace the floppy disk drive (see Figures 6-5 and 6-6):

1. Turn off the Series 2000 power and unplug the AC power cord. (See "Controls, Connectors, and Indicators" in **System Description** - Chapter 1 for the locations of the power switch and power cord connector.)

2. Position the floppy drive with the mounting bracket facing down.

3. Connect the 4-pin power cable connector to the corresponding connector on the back of the drive. (The connector is keyed for the proper orientation.)

4. Connect the 25-pin connector to the corresponding connector on the back of the drive as shown in Figure 6-6. Do not twist the cable -- keep the red cable stripe to your right as you face the back of the system.

5. Install the steel dust cover by placing one end into the grooves at the cable end and pulling the other end over until it pops into place.

6. Slide the drive into the chassis. Guide the cables back into the chassis as you slide the drive into the slot.

7. Gently press the drive until it seats firmly in the chassis.

8. Use a #2 Phillips screwdriver to press in and turn the locking screw a 1/4-turn clockwise as shown in Figure 6-5.

9. Replace the front panel in the reverse order of removal.

Removing the Hard Disk Drive

Perform the following procedure to remove the hard disk drive (see Figures 6-7 and 6-8):

1. Turn off the Series 2000 power and unplug the AC power cord. (See "Controls, Connectors, and Indicators" in **System Description** - Chapter 1 for the locations of the power switch and power cord connector.)

2. Remove the front panel as described previously.

CAUTION

The hard disk drive is sensitive to shock and vibration. Do not drop or jar the drive. Wait at least 30 seconds after powering off the system before removing a hard disk drive.

3. Unplug the small AC connector located near the upper right corner of the hard disk drive by pressing down on the latch as shown in Figure 6-7.

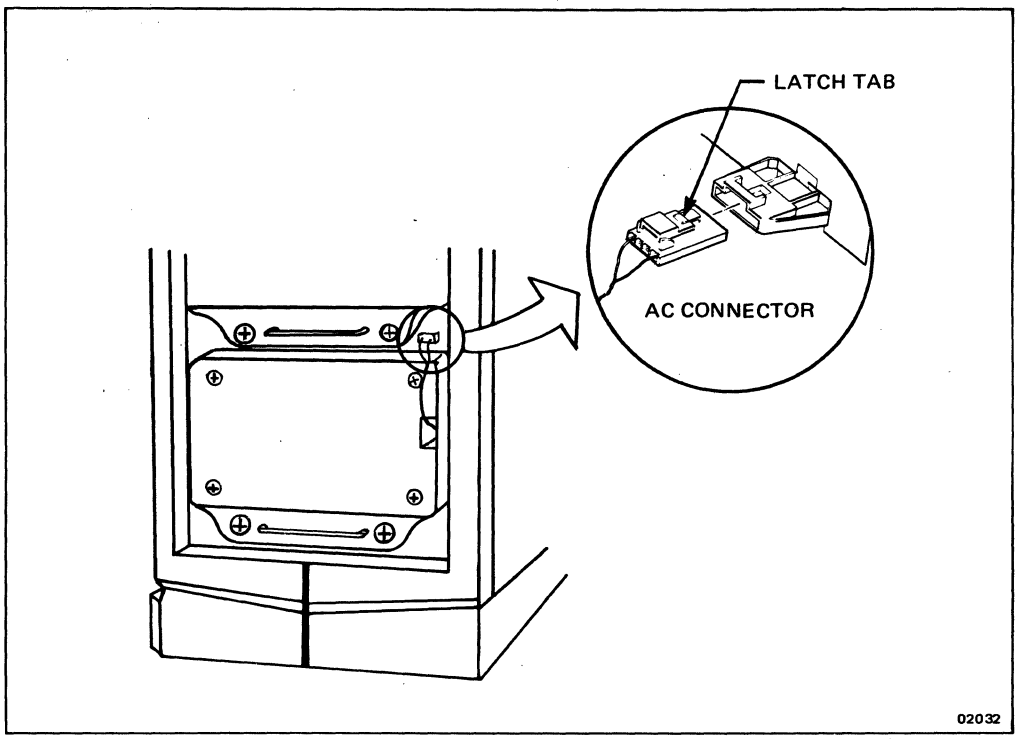


Figure 6-7. Removing/Replacing the Hard Disk AC Connector

4. Use a #2 Phillips screwdriver to turn the two screws on the drive mounting bracket a 1/4-turn counterclockwise as shown in Figure 6-8.

5. Grasp the handle and pull it toward you to slide the drive out of the chassis.

6. Replace the hard disk drive as described in the following procedure.

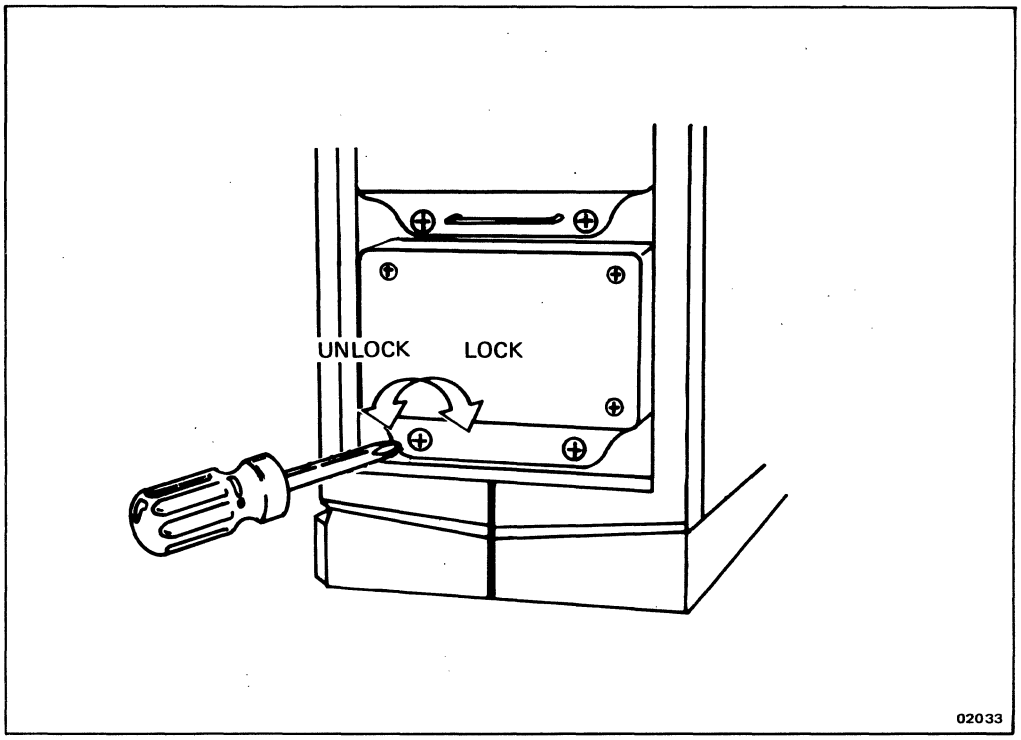


Figure 6-8. Unlocking/Locking the Hard Disk Drive Mounting Screws

Replacing a Hard Disk Drive

Perform the following procedure to replace a hard disk drive (see Figures 6-7 and 6-8):

1. Turn off the Series 2000 power and unplug the AC power cord. (See "Controls, Connectors, and Indicators" in **System Description** - Chapter 1 for the locations of the power switch and power cord connector.)

2. Remove the front panel as described previously.

CAUTION

The hard disk drives are sensitive to shock and vibration. Do not drop or jar a drive. Wait at least 30 seconds after powering off the system before replacing a hard disk drive.

NOTE

Hard disk drives are installed from the bottom up. If there is one hard disk drive, install it in the bottom slot. If there are two hard disk drives, install them in the bottom two slots. If there are three hard disk drives, install one drive in each of the available hard disk slots.

3. Position the drive with the handle and mounting bracket on the bottom. Place the flanged sides of the drive into the grooves of the correct drive slot.

4. Press evenly against the front of the drive until it is completely seated in the slot.

5. Use a #2 Phillips screwdriver to turn the two screws on the mounting bracket a 1/4-turn clockwise as shown in Figure 6-8.

6. Plug the hard disk AC connector into the corresponding connector located in the upper right-hand corner of the drive slot as shown in Figure 6-7.

7. Replace the front panel in the reverse order of removal.

Removing the Plug-In Printed Circuit Boards

Perform the following procedure to remove/replace the plug-in boards (see Figure 6-9):

1. Turn off the Series 2000 power and unplug the AC power cord. (See "Controls, Connectors, and Indicators" in **System Description** - Chapter 1 for the locations of the power switch and power cord connector.)

2. Grasp each board-extractor ring located at the bottom and top of the board.

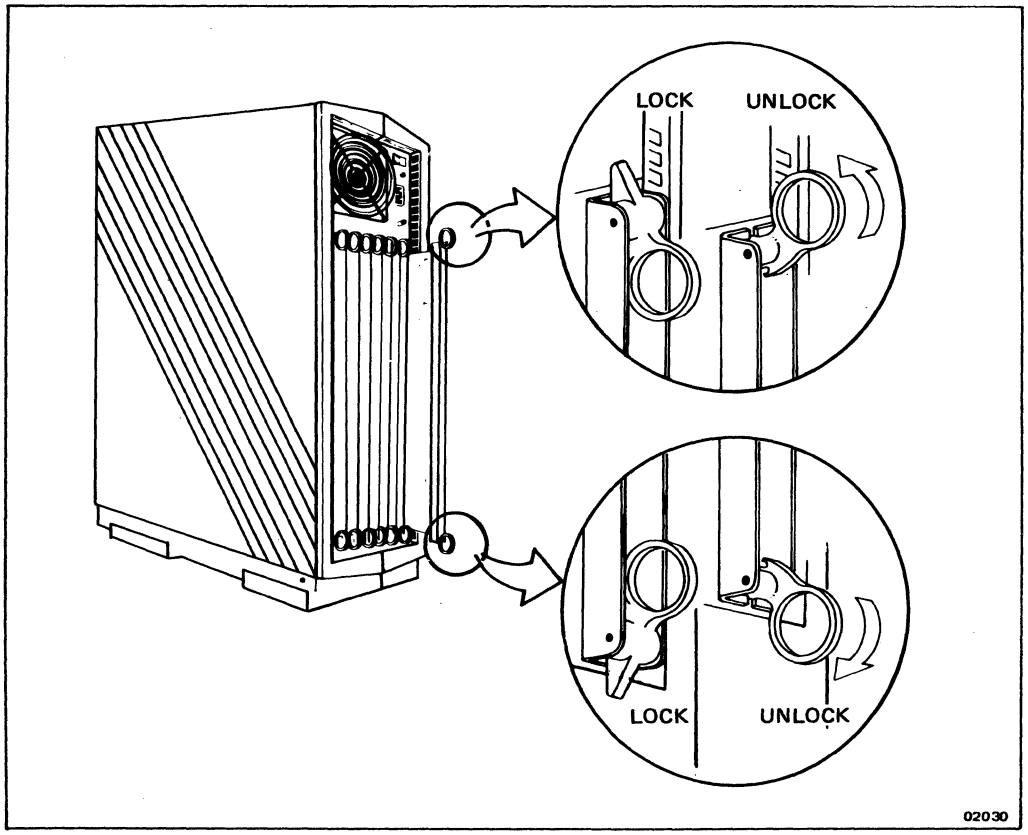


Figure 6-9. Removing/Replacing the Plug-In Boards

3. Gently pull straight out on both extractor rings simultaneously and slide the board out of the chassis.

4. Replace the board by positioning both extractor rings straight out from the channel bracket. Slide the board part way into the appropriate slot and push firmly in the center of the channel bracket. The extractor rings should automatically lock the board in place.

However, make sure that the boards are locked in place by pressing the extractor rings down tight against the board channel bracket.

Removing the Main Power Supply

Perform the following procedure to remove/replace the main power supply (see Figure 6-10):

1. Turn off the Series 2000 power and unplug the AC power cord. (See "Controls, Connectors, and Indicators" in **System Description** - Chapter 1 for the locations of the power switch and power cord connector.)

2. Remove the front panel as described previously.

3. Remove the left-hand side panel as described previously.

4. Disconnect the power supply harness connector from the backplane board and the power connector from the fan. (If there are three hard disk drives installed, remove the top drive to gain access to the power supply harness connector.)

5. Use a #2 Phillips screwdriver to remove the four screws securing the main power supply board to the chassis as shown in Figure 6-10. (The power on/off switch, line-voltage receptacle, and fuse holder are removed with the power supply.)

6. Slide the power supply toward the front of the chassis, then tilt the back of the power supply up and remove.

7. Replace the main power supply board in the reverse order of removal. Make sure that the grounding washers are properly installed.

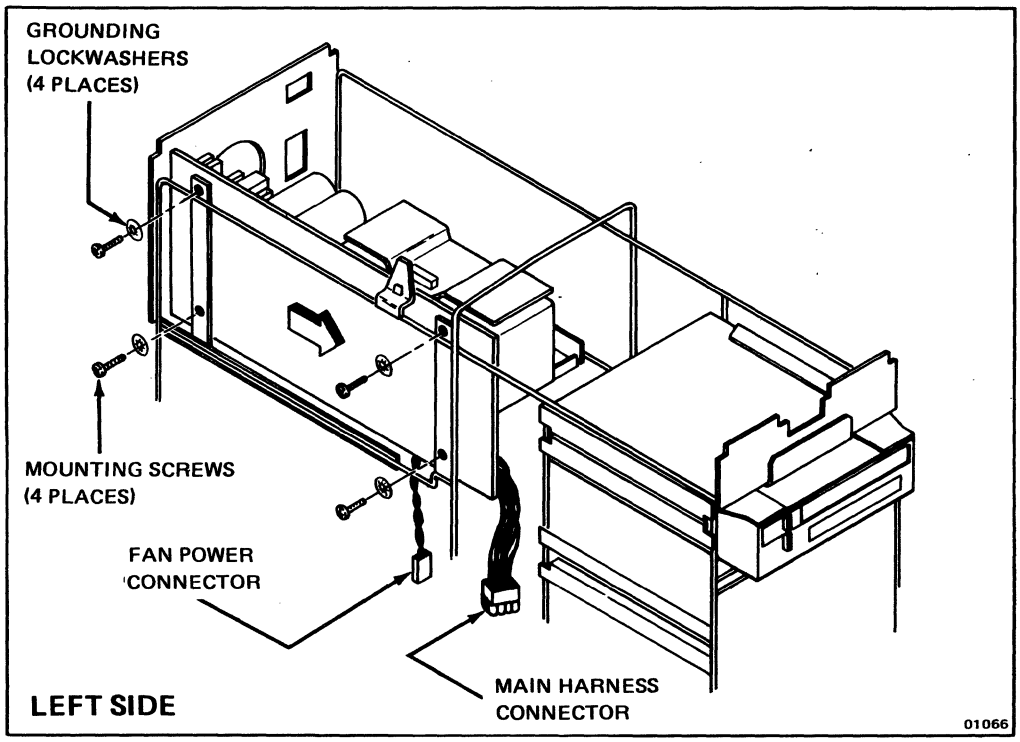


Figure 6-10. Removing/Replacing the Main Power Supply

Removing the Backplane Board

Perform the following procedure to remove/replace the backplane board (see Figure 6-11 and 6-12):

1. Turn off the Series 2000 power and unplug the AC power cord. (See "Controls, Connectors, and Indicators" in **System Description** - Chapter 1 for the locations of the power switch and power cord connector.)

2. Remove the front panel as described previously.

3. Remove the right-hand side panel as described previously.

4. Remove the cartridge tape, floppy, and hard disk drives as described previously.

5. Remove the plug-in boards as described previously.

6. Unplug the harness connectors from the backplane board.

7. Use a #2 Phillips screwdriver to remove the three top and three bottom screws and washers securing the backplane board with its mounting frame to the chassis as shown in Figure 6-11.

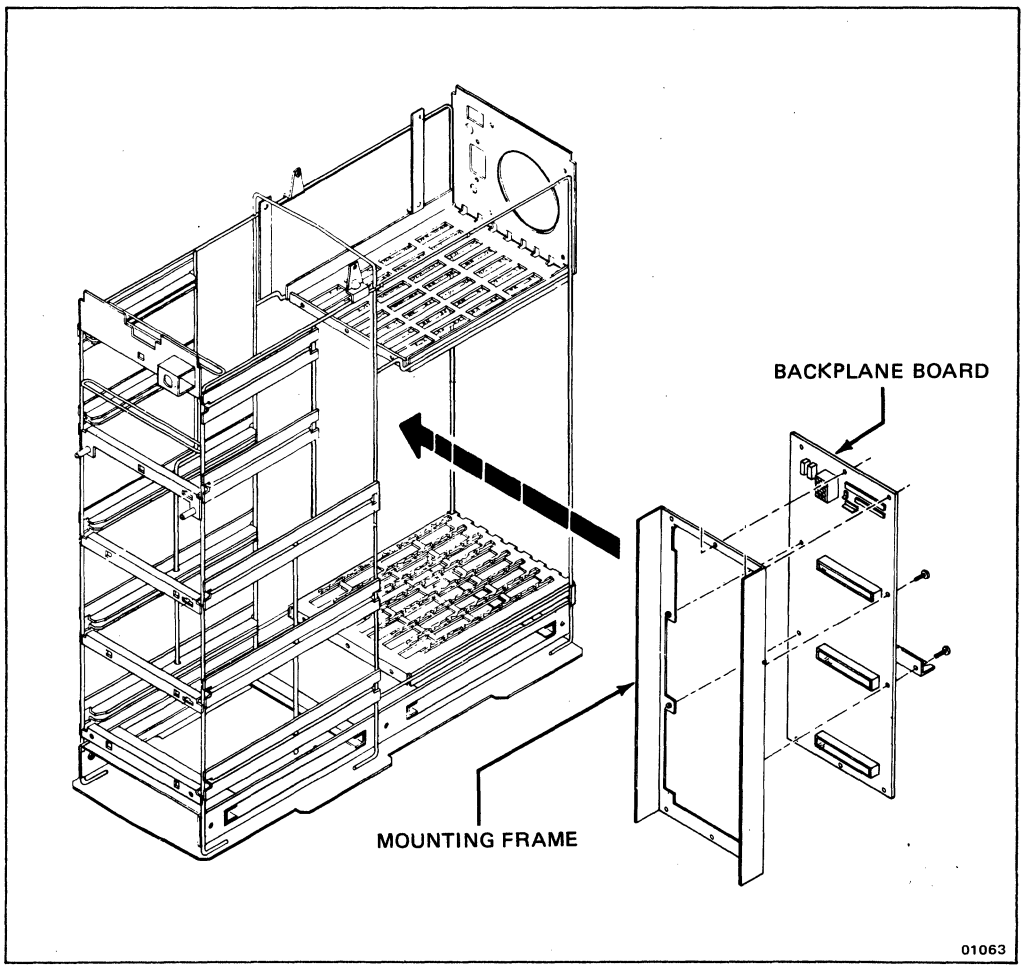


Figure 6-11. Removing/Replacing the Backplane Board

8. Gently lift the backplane board up and slide it out from the right-hand side of the cabinet.

9. Use a #2 Phillips screwdriver to remove the four screws and washers securing the backplane board to the mounting frame.

10. Replace the backplane board in the reverse order of removal. Make sure that all the mounting washers are properly installed and that the harness connectors are attached to the proper backplane board connectors. Refer to Figure 6-12 for the proper cable connections to the backplane board.

Removing the LED Board

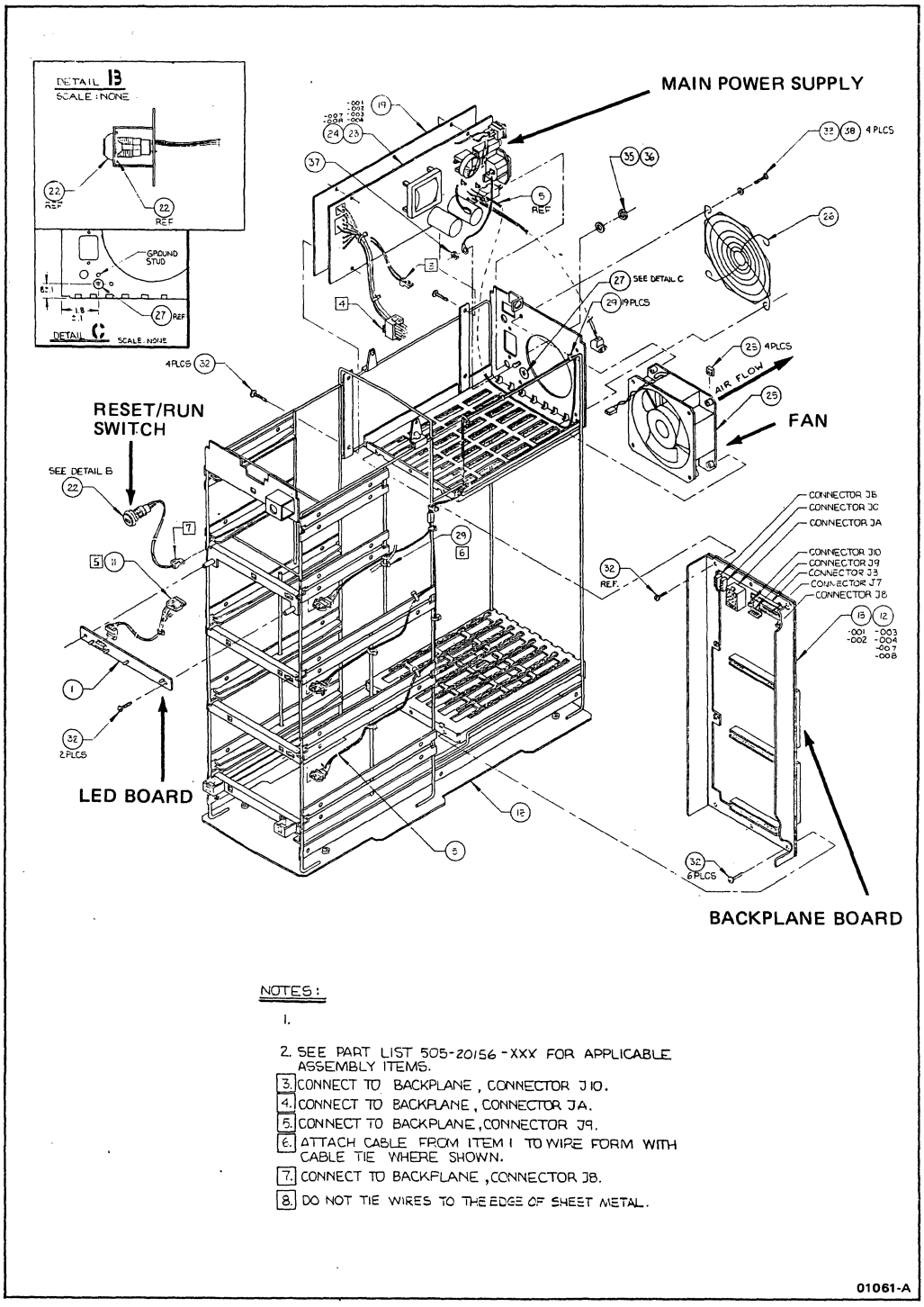
Perform the following procedure to remove/replace the light-emitting diode (LED) board:

1. Remove the front panel as described previously.

2. Disconnect the harness connector from the LED board.

3. Use a #2 Phillips screwdriver to remove the two screws securing the LED board to the chassis.

4. Replace the LED board in the reverse order of removal.



NOTES:

1.

2. SEE PART LIST 505-20156-XXX FOR APPLICABLE ASSEMBLY ITEMS.
3. CONNECT TO BACKPLANE, CONNECTOR J10.
4. CONNECT TO BACKPLANE, CONNECTOR JA.
5. CONNECT TO BACKPLANE, CONNECTOR J9.
6. ATTACH CABLE FROM ITEM 1 TO WIRE FORM WITH CABLE TIE WHERE SHOWN.
7. CONNECT TO BACKPLANE, CONNECTOR J8.
8. DO NOT TIE WIRES TO THE EDGE OF SHEET METAL.

Figure 6-12. Cable Interconnections

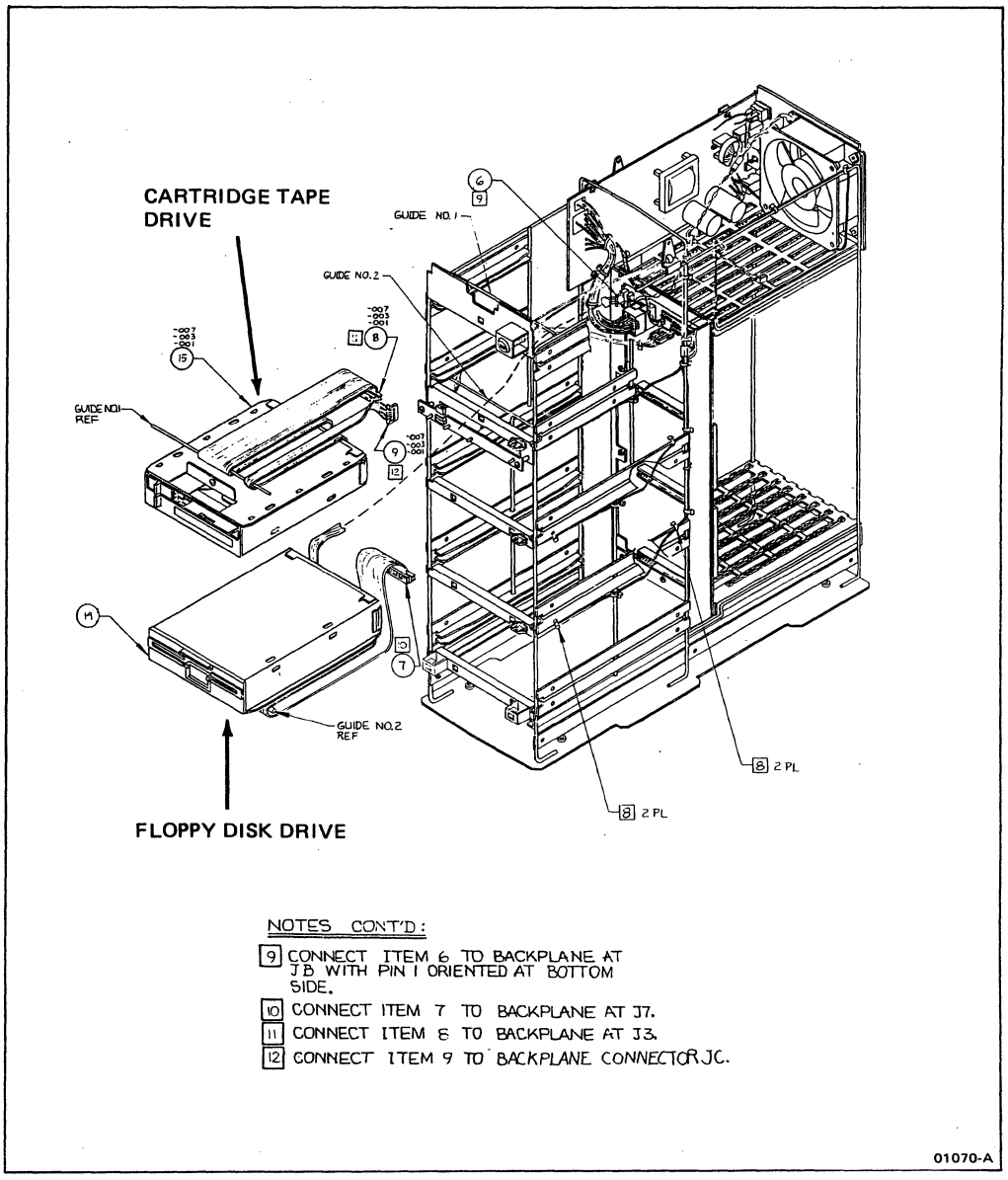


Figure 6-12. Cable Interconnections (Cont.)

SHIPPING A FIELD-REPLACEABLE UNIT

Always contact Altos Customer Service before returning a unit for factory service. If service is required, a customer service technician will assign you a Return Authorization (RA) number.

Do not send in a unit for repair without an RA number. Also supply the following:

- model number of your system
- serial number of your system
- date purchased or sent for service
- specific problem
- name, address and telephone/telex number of your company and name of a responsible technical person whom Altos service may contact if necessary

CAUTION

Make sure you back up any hard disk data you wish to save before sending the hard disk drive for repair. The test procedure destroys the data on the hard disk. Altos cannot guarantee the integrity of data on hard disks which are sent for repair.

Packaging the System Unit

Use the original shipping container and packing if possible. If you do not have an Altos container, contact your dealer to see if one is available. If you still cannot obtain the correct container, ship the unit in a foam-padded heavy-duty corrugated shipping carton. Place a head protection sheet (shipped with the floppy drive) over the drive heads. Seal the carton securely and mark it FRAGILE. Remember to write the Return Authorization (RA) number on the outside and to insure the package. Altos cannot be responsible for lost or damaged shipments.

Packaging Storage Devices

For best results, package tape, floppy disk, or hard disk drives in a sturdy foam-padded shipping carton if you do not have Altos packaging.

If you are shipping a floppy drive, insert a head protection sheet over the drive heads. Seal the carton securely and mark it FRAGILE. Remember to write the Authorization number on the outside and to insure the package. Altos cannot be responsible for lost or damaged shipments.

Packaging Printed Circuit Boards

If you are shipping a printed circuit board and you do not have Altos packaging, wrap the unit in an anti-static cushioning material (such as Air Cap TH-240 available from Sealed Air Corporation, Hawthorne, New Jersey). Do not package boards using foam padding. Enclose the board in a heavy-duty corrugated shipping carton. Seal the carton securely and mark it FRAGILE. Remember to write the Return Authorization (RA) number on the outside and to insure the package. Altos cannot be responsible for lost or damaged shipments.

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Chapter 7
Preventive Maintenance

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INTRODUCTION

This chapter includes preventive maintenance information which consists of cleaning the dust filters, the cabinet exterior, the interior electrical components, and the cartridge tape and floppy disk drives.

NOTE

Altos recommends that the procedures in this chapter be performed by qualified service personnel.

CLEANING

To assure maximum trouble-free operation, regular preventive maintenance should be performed. Dust accumulation on the electrical components can act as a heat-insulating blanket or create an electrical conduction path that can cause component failure. A coating of dust and tape particles can accumulate on the tape heads and cause faulty tape operation.

The following preventive maintenance should be performed at the specified intervals:

- dust filters should be cleaned at least every three months
- cartridge tape heads should be cleaned after initial pass of a new cartridge or each eight hours of tape contact
- interior electrical components should be visually inspected and cleaned at least every six months or as often as operating conditions require
- floppy disk head assembly should be cleaned and belts checked every 12 months

WARNING

Dangerous potentials exist inside the cabinet. Turn off the Series 2000 power and unplug the AC power cord before performing the following preventive maintenance procedures.

Perform the following procedures to clean the filters, the exterior and interior components, and the cartridge tape and floppy disk heads. Altos does not recommend that the hard disk drive(s) be removed or disassembled for cleaning.

CAUTION

Do not use chemical or abrasive cleaning agents that can damage the plastics used in the component parts of the system.

Dust Filters

A #1 or #2 Phillips screwdriver and some mild household detergent are required to clean the dust filters. (Order an extra set of filters so you always have clean filters available.)

Perform the following procedure to remove and clean the dust filters (see Figures 7-1 and 7-2):

1. Turn off the Series 2000 power and unplug the AC power cord. (See "Controls, Connectors, and Indicators" in **System Description** - Chapter 1 for the locations of the power switch and power cord connector.)

2. Remove the cabinet front panel as described in **Removal/Replacement** - Chapter 6.

3. Grasp one corner of the filter located behind the front panel and pull it toward you until all velcro pads are released.

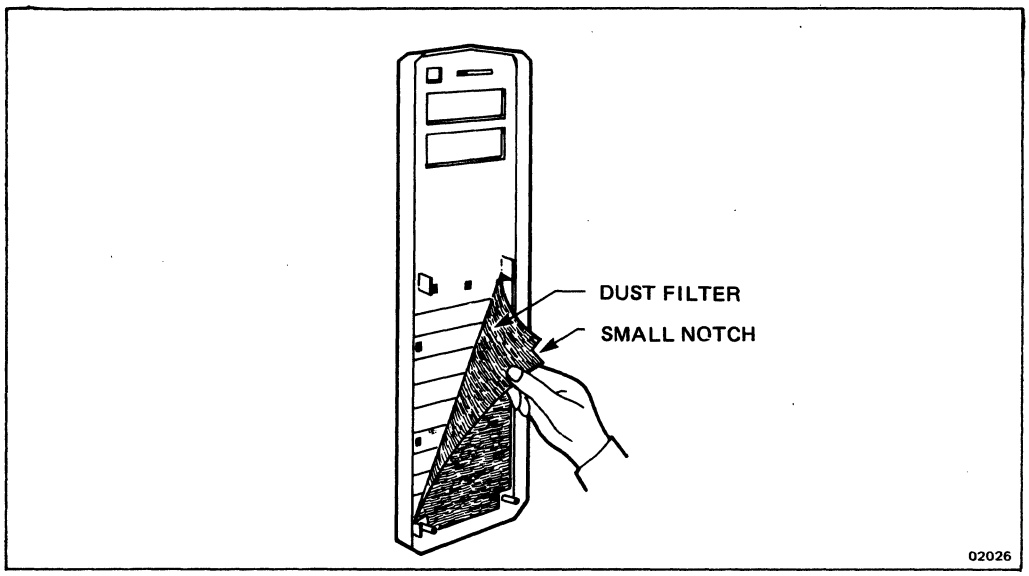

Figure 7-1. Removing/Replacing the Front Panel Filter

4. Pull the filter located under the bottom hard disk drive toward you until it comes completely out of the chassis.

5. Clean the filters by soaking them in a mild solution of water and household detergent. Rinse them thoroughly with clean water. Gently pat the filters with a dry towel to remove excess water, but do not twist or bend them.

CAUTION

Let the filters dry for at least six hours before replacing them in the chassis. Never install damp filters in the cabinet!

6. Replace the front filter with the smooth side up. Press firmly on the velcro pads to secure the filter. Slide the bottom filter into its rails at the bottom of the chassis.

7. Replace the front panel in the reverse order of removal.

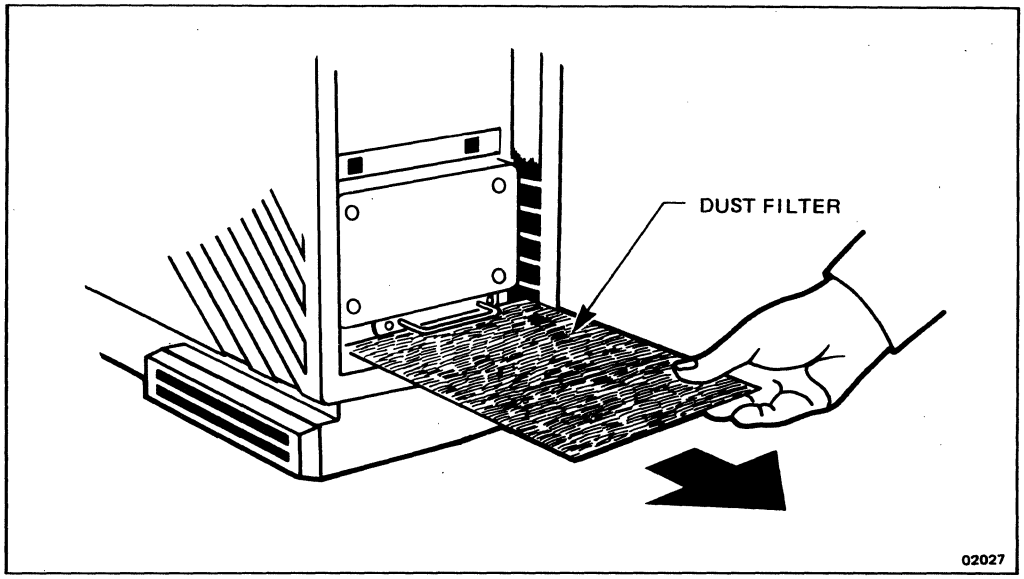

Figure 7-2. Removing/Replacing the Bottom Filter

Tape Heads

The cartridge tape drive read/write/erase heads should be cleaned and the soft error statistics checked to determine tape or tape drive deterioration after every eight hours of actual tape motion. Read or write error statistics are available to the operating system through the Read Status command. The Read Status command should be executed after each cartridge is used.

The drive should also be cleaned after an initial pass of a new cartridge or, if only new cartridges are used, after every eight hours of tape motion.

The recommended method for cleaning is to use a cartridge cleaner kit, available from electronics suppliers. An alternative method is to gently wipe the head area with a six-inch long cotton swab lightly dipped in a 95% isopropyl alcohol solution or standard tape head cleaning solution (Miller-Stephenson MS-200 or equivalent).

While this alternative method is acceptable when a cleaning cartridge is not available, it is more likely to leave an unwanted residue in the head area. Ensure that drive power is off when applying an alcohol or head cleaning solution.

Perform the following procedure to clean the tape heads (see Figure 7-3):

1. Remove the tape cartridge from the drive by moving the lever to the left. If your drive does not have a lever, press in on the cartridge to release the tape.

2. Expose the tape heads by pressing the tape lever to the right, if you have a lever-style drive. If you do not have a lever, press in firmly on the plate at the bottom of the tape slot. When you press in on the bottom plate, the tape head assembly pops out.

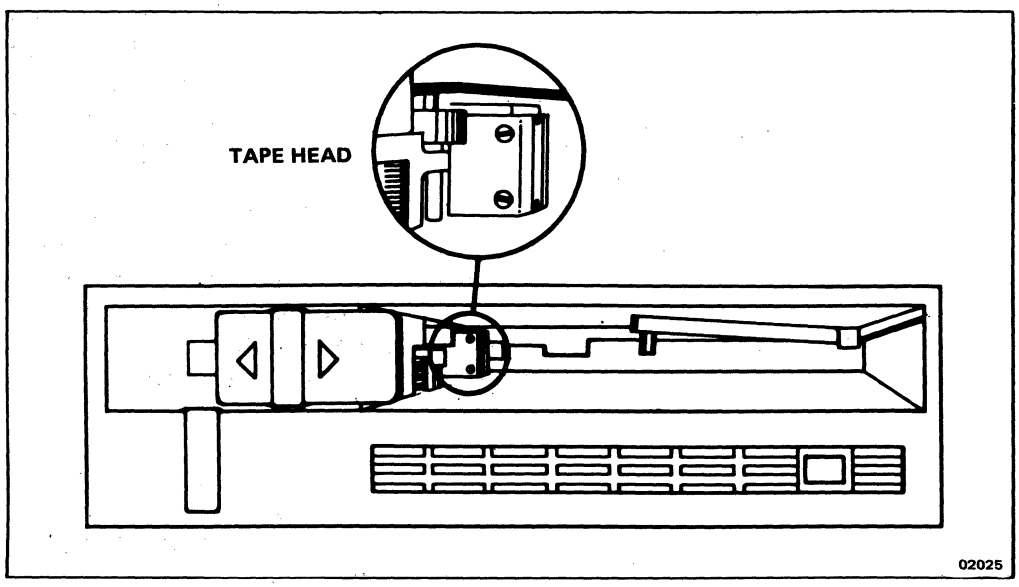

Figure 7-3. Cleaning the Tape Head

3. Dip the cotton swab in the cleaning solution.

4. Gently wipe the brass and porcelain parts of the head assembly.

5. Use a dry swab to wipe off any excess solution.

CAUTION

Make sure you allow the heads to dry completely before using the tape drive.

6. If you have a lever-type unit, move the lever to the left. If you pressed in on the bottom plate to expose the tape heads, press in on the plate again until it clicks back into place.

Floppy Disk Drive

The floppy disk drive belt and disk head drive should be checked and the head and pressure pad assembly cleaned every 12 months in average use and dust environments. The frequency of preventive maintenance depends entirely on the amount of use and, most important, on the amount of dust in the operating environment. The head and pressure pad assembly are the most critical parts to maintain.

A cleaning disk for floppy disk drives is the recommended method for cleaning the head and pressure pad assembly. If read/write problems persist, it may be necessary to remove and disassemble the drive, clean the head, and replace the pressure pad. **(This should only be done by qualified service personnel.)** Refer to the appropriate floppy disk drive service manual for detailed procedures.

Check the belt for excessive wear and the disk head drive assembly for proper alignment. Head alignment should only be attempted by qualified service personnel. Refer to the appropriate floppy disk drive service manual for detailed procedures.

Exterior

Use a soft-bristled brush or soft cloth to remove loose dust or foreign material from the side panels and exterior of the cabinet.

Stubborn dirt can be removed with a soft cloth dampened with a mild solution of non-abrasive household detergent and water.

Interior

Check the interior of the cabinet for dust or dirt accumulation (especially on the electrical components). If there is visible dust or dirt accumulation on the interior components, clean as described in the following procedure:

1. Turn off the Series 2000 power and unplug the AC power cord. (See "Controls, Connectors, and Indicators" in **System Description** - Chapter 1 for the locations of the power switch and power cord connector.)

2. If applicable, remove the cabinet side panels as described in **Removal/Replacement** - Chapter 6.

3. Remove the printed circuit boards as described in **Removal/Replacement** - Chapter 6.

4. Use low-velocity air (approximately 5 psi) or a soft-bristled brush to remove loose dust from the interior of the cabinet and from the boards.

   A cotton-tipped applicator is useful for cleaning in narrow spaces. Be careful when cleaning around electrical components.

5. Replace the boards and side panels in the reverse order of removal.

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Appendix A
Jumper and Switch Settings

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INTRODUCTION

This appendix describes the proper jumpering for the Series 2000 memory, communications (multidrop and SIO), and CPU printed circuit boards and also the switch settings for the terminal cluster unit (TCU). The following information is included:

- when to change the memory and communications jumpers
- how to set the memory board jumpers
- how to set the communications board jumpers
- how to select the recommended slot for a memory or communications board
- how to set the terminal cluster unit (TCU) switches
- default (shipping) jumper settings for the CPU board

NOTE

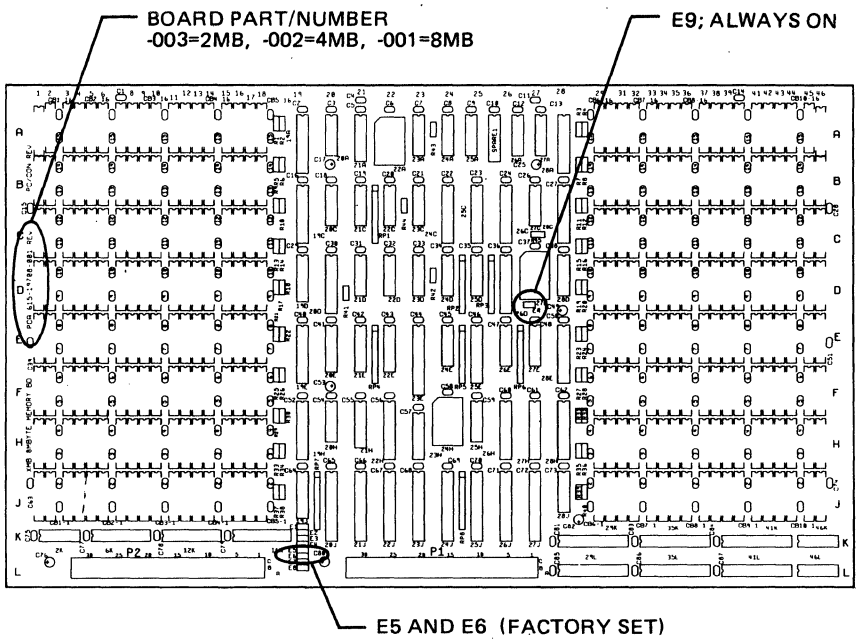
Installing TCUs with incorrect station address switch settings or memory and communications boards with incorrect jumper settings will not damage the equipment, but the multidrop system will not operate properly.

The jumpers were placed in the correct positions and the boards were installed in the recommended slots when the Series 2000 was shipped from the factory. Check and possibly move jumpers when you replace the memory or communications boards, or when you install additional memory or communications boards.

MEMORY BOARD JUMPERS

When you replace or add a memory board, check and possibly change the jumpers. The jumpers select which memory addresses each board will decode. The memory address spaces must be contiguous (the addresses on the second board must start where the addresses on the first board end, etc.). In addition to checking the jumpers, check that the memory board with the largest memory capacity (for example 8M bytes) is installed in slot B, the next largest memory capacity (for example, 4M bytes) in slot C, down to the memory board with the smallest capacity. Using the recommended slots substantially reduces troubleshooting time during diagnostic testing.

In order for the system to work properly, *each* memory board must be jumpered with: (1) the board number and (2) the size (memory capacity) of the board. Figure A-1 illustrates the E5 and E6 default (factory) jumper settings for the memory board series.



PART NUMBER	SIZE	SETTING
6X5-19708-003	2MB	E5 ON; E6 ON
-002	4MB	E5 ON; E6 OFF
-001	8MB	E5 OFF; E6 OFF

ON= JUMPER INSTALLED
OFF= JUMPER NOT INSTALLED

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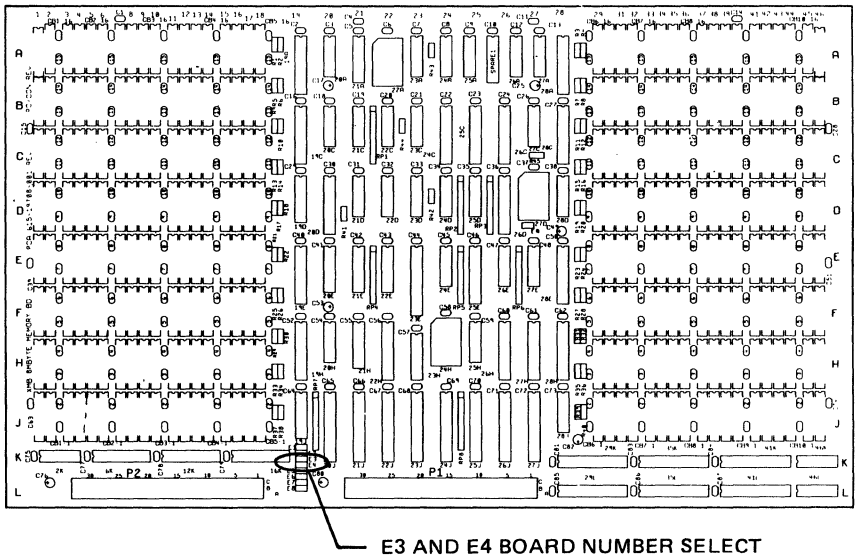
Figure A-1. Default Jumper Settings

Figure A-2 illustrates the E3 and E4 jumper settings for the memory board series (version -001 is 8M bytes, -002 is 4M bytes, and -003 is 2M bytes). The E3 and E4 setting tells your system whether the board is the first (board 0), second (board 1), or third (board 2) memory board.



BOARD NUMBER	SETTING
0 (FIRST MEMORY EXPANSION)	E3 ON; E4 ON
1 (SECOND MEMORY EXPANSION)	E3 ON; E4 OFF
2(THIRD MEMORY EXPANSION)	E3 OFF; E4 ON

ON= JUMPER INSTALLED
OFF= JUMPER NOT INSTALLED

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Figure A-2. Board Number Jumper

Tables A-1 through A3 summarize the jumper settings for an 8M, 4M, and 2M byte memory board installed as board 0, 1, or 2. Figure A-3 illustrates the jumper settings for *each* new version memory board you install.

Table A-1. Jumpers For 8M Byte Memory Boards Installed As Board 0, Board 1, Or Board 2

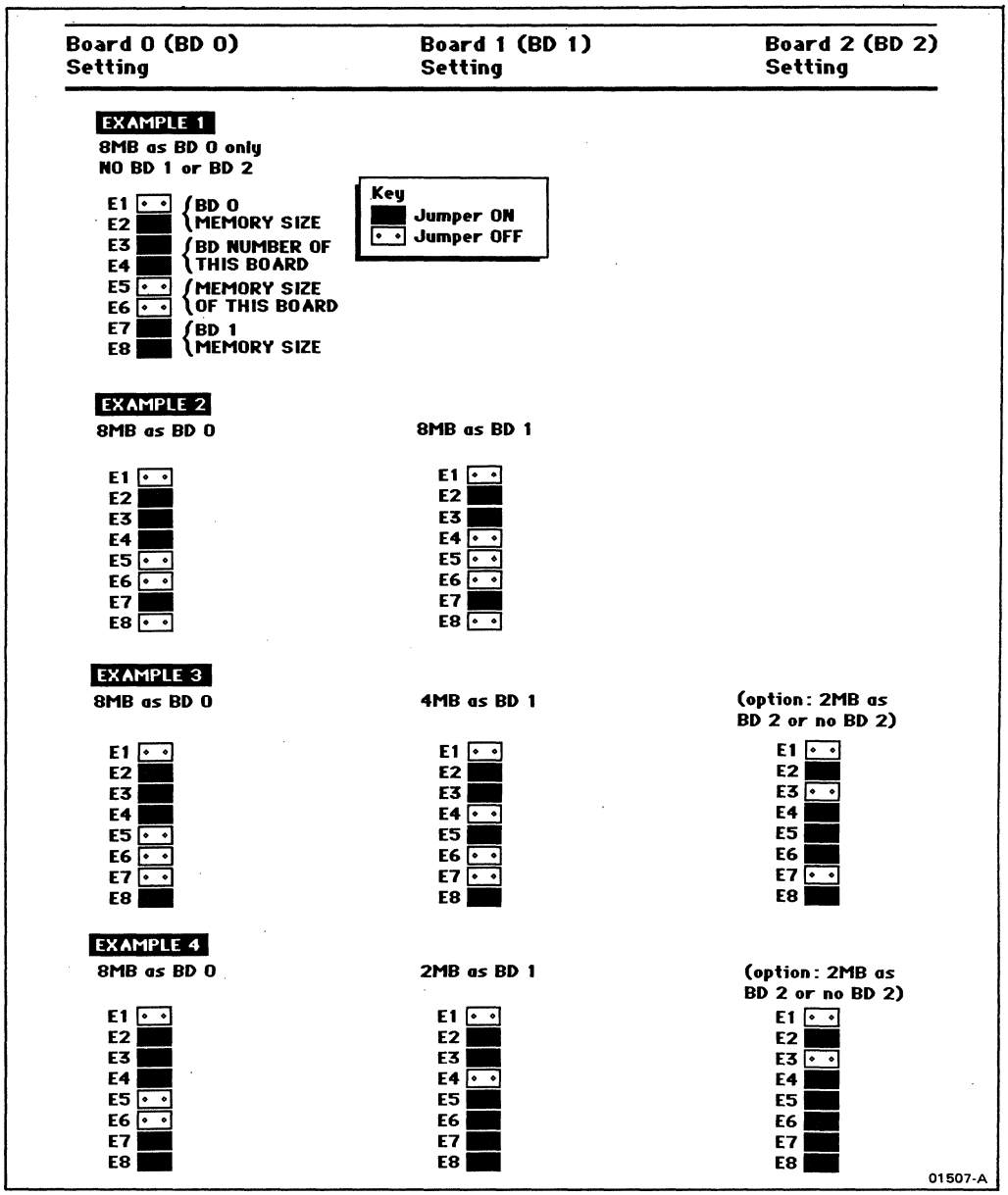


Table A-2. Jumpers For 4M Byte Memory Boards Installed As Board 0, Board 1, Or Board 2

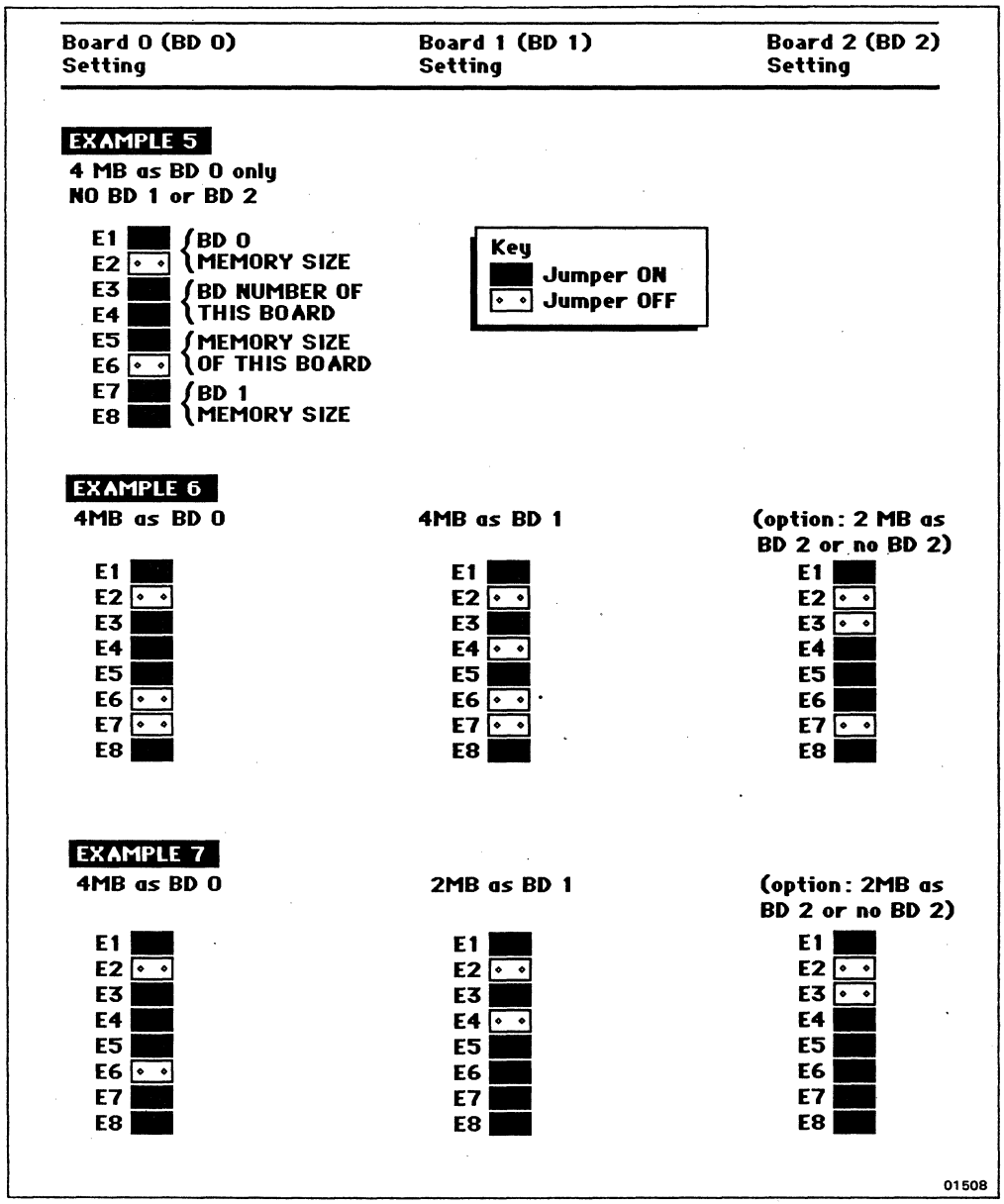


Table A-3. Jumpers For 2M Byte Memory Boards Installed As Board 0, Board 1, Or Board 2

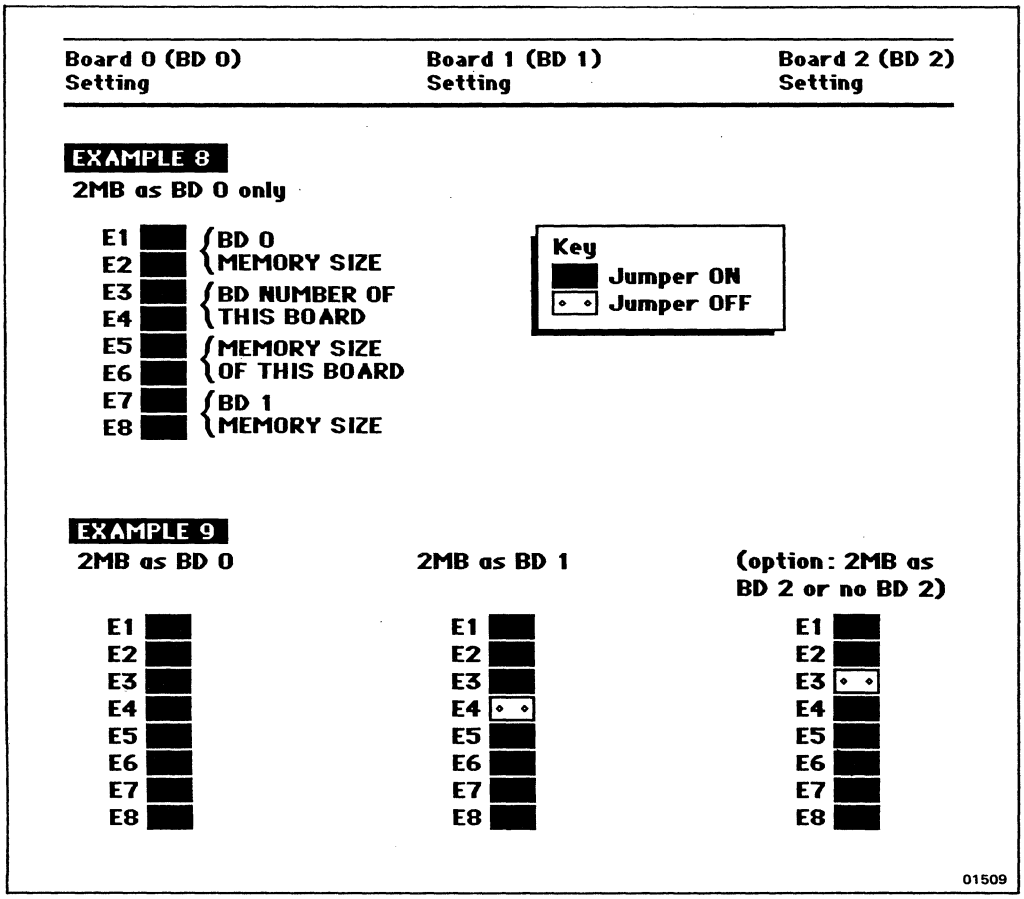
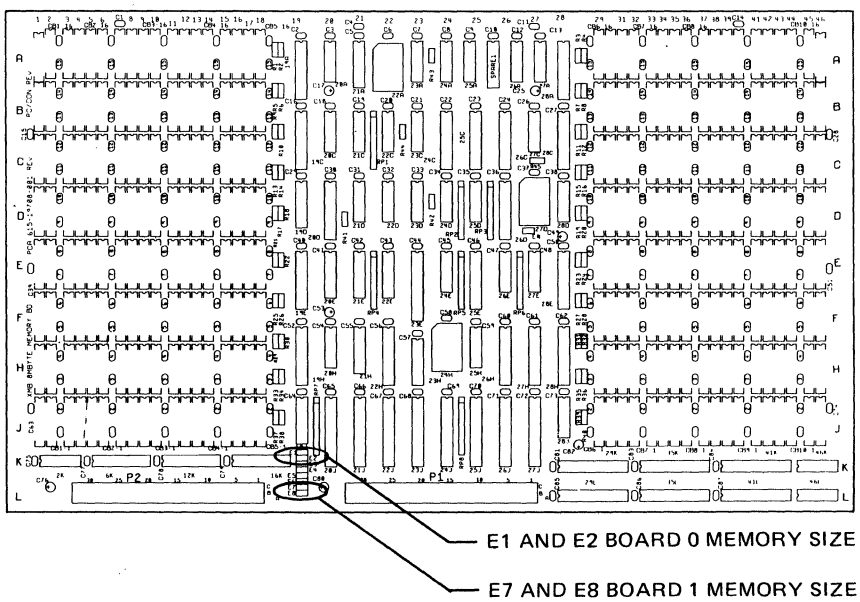


Figure A-3 illustrates the board 0, and board 1 memory size jumpers which must be installed on *each* memory board in the system. Although you do not set the size of board 2 on any of the boards, you do have to set the size of boards 0 and 1 on board 2.

NOTE

If you only have one board, use the 2M byte board setting for board 1.



BOARD 0 MEMORY SIZE	BOARD 1 MEMORY SIZE
BOARD 0= 2MB E1 ON; E2 ON	BOARD 1*= 2MB E7 ON; E8 ON
BOARD 0= 4MB E1 ON; E2 OFF	BOARD 1= 4MB E7 OFF; E8 ON
BOARD 0= 8MB E1 OFF; E2 ON	BOARD 1= 8MB E7 ON; E8 OFF

*OR NO SECOND BOARD

ON= JUMPER INSTALLED
OFF= JUMPER NOT INSTALLED

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Figure A-3. Memory Configuration Jumpers on Board 0, Board 1, And Board 2

Figure A-4 shows an example of a system with one 2M byte (version -003), one 4M byte (version -002), and one 8M byte (version -001) board.

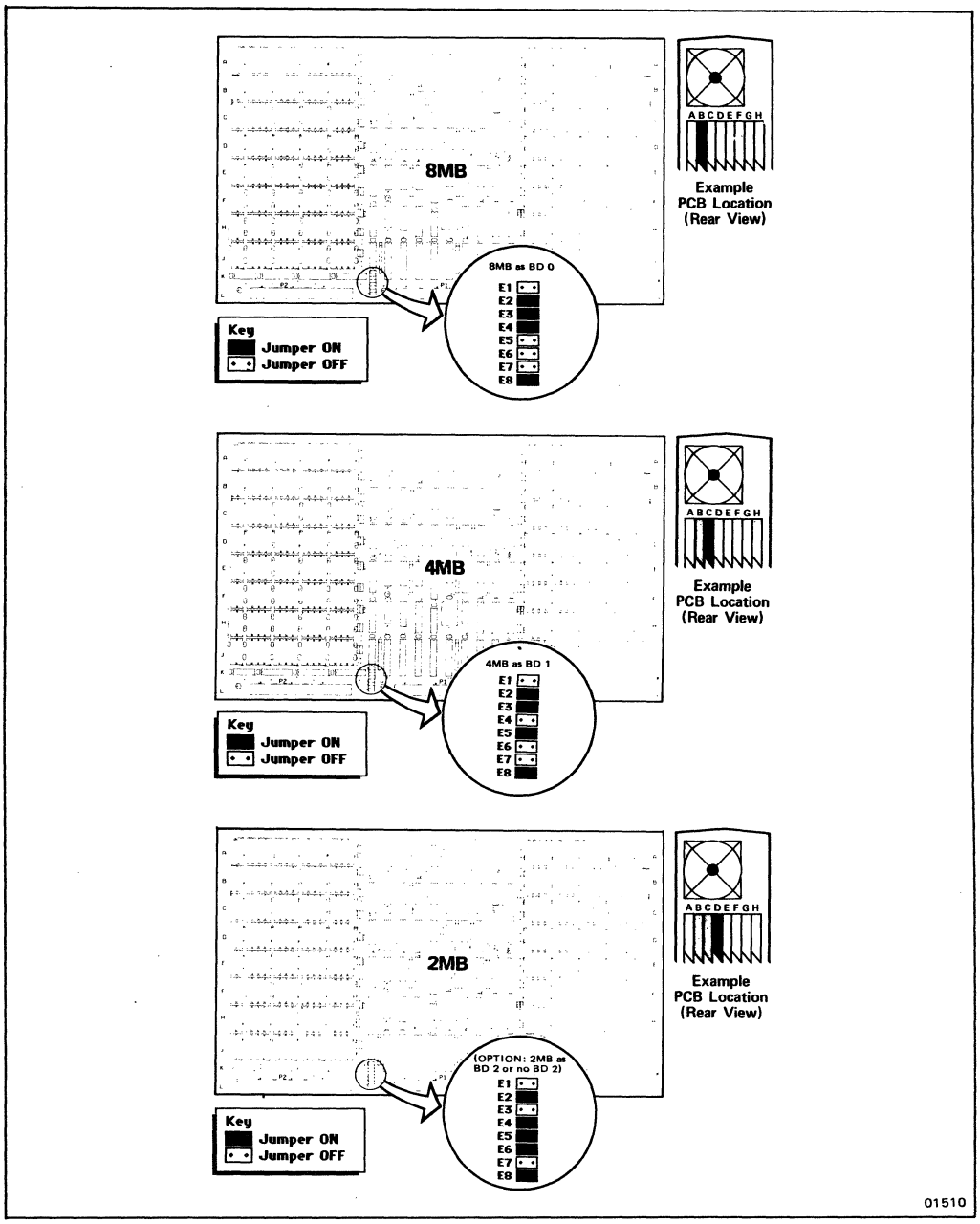


Figure A-4. An Example Memory Configuration

COMMUNICATIONS BOARD JUMPERS

Slots C through F in the back of the Series 2000 accommodate multidrop and/or SIO communications board(s). The primary communications board, with the console/boot port, is designated as COMM 0 and is always installed in slot F. The secondary communications board(s) are designated COMM 1 through 3 and are assigned to slots E, D, and C respectively.

Both multidrop and SIO communications boards can be jumpered to function as primary or secondary boards. (However, it is recommended that a multidrop communications board, jumpered as the primary board, be installed in slot F.)

Each communications board must be jumpered according to its logical location in the system. (Refer to "Plug-In Printed Circuit Board Locations" in **System Description** - Chapter 1 for additional location information.)

Before you replace, add, or change a communications board, check and possibly change the jumpers. The following jumper descriptions include the proper jumper connections for multidrop and SIO communications boards used as primary or secondary devices.

Multidrop Communications Board Jumpers

The multidrop communications (MDC) board has nine jumper connectors that are used to select the options described in Table A-4. Table A-5 describes additional functions for jumpers E5 through E8. Figures A-5 through A-9 illustrate the proper jumper connections and recommended slot locations for primary and secondary MDC boards.

Table A-4. Multidrop Board Jumper Descriptions

Connector Designation	Description
E2 (1-2)	Use determined by software. Currently undefined
E2 (3-4)	Jumper installed identifies this communications board as the primary board with the boot port
E2 (5-6)	Jumper installed causes the IPL PROM to go into a stand-alone mode after reset. This jumper is not normally installed (used for debugging)
E3 (1-2)	Local Reset. For debug use only. Forces a reset on the multidrop board ONLY (does not reset any other board in the system). Normally not jumpered
E4 (1-2)	Jumper installed only if type 27256 PROMs are used. Normally not jumpered
E5 E5-1 to -16	CHANATTN (Channel Attention). Selects system I/O port address that this board will recognize as a channel attention interrupt from another bus master. Jumper position is system dependent
E6 E6-1 to -16	BPN (Bus Priority Input). Used to determine the arbitration priority when the multidrop board wishes to access the system bus. MUST be jumpered the same as BRQ. BPN-0 (E6 pins 15 and 16) is the highest priority. Jumper position is system dependent
E7 E7-1 to -16	BRQ (Bus Request). See BPN above
E8 E8-1 to -16	SYSINT (System Interrupt). Selects the interrupt vector level that this board will generate to the system CPU. INT-0 (E8 pins 15 and 16) is the highest priority. Jumper is system dependent
E9 (1-2)	Normally jumpered. Enables the master oscillator

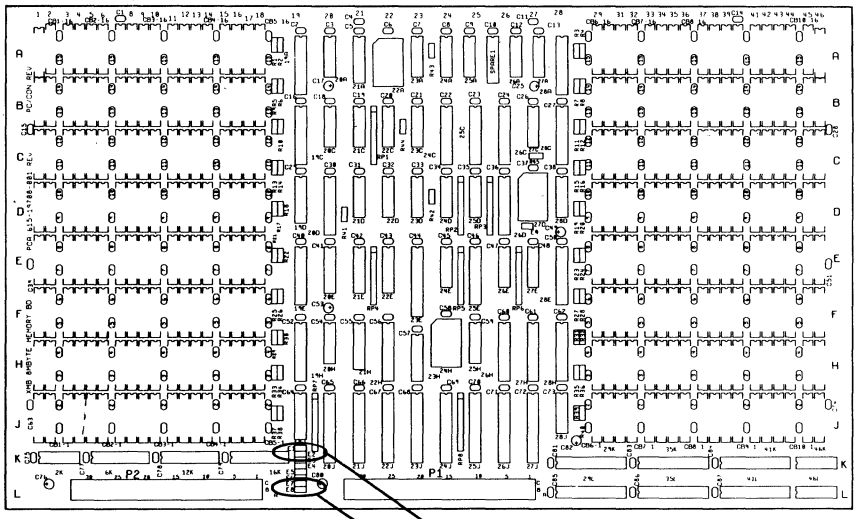
Table A-4. Multidrop Board Jumper Descriptions (Cont.)

Connector Designation	Description
E-9 (3-4)	Normally open. Enables the 6.144 MHZ SCC clock oscillator
E9 (5-6)	Normally jumpered. Derives the SCC clock from the master oscillator
E9 (7-8)	Normally jumpered. Enables the 19.6608 MHz oscillator
E9 (9-10)	Normally open. Changes the refresh counter and SCC recovery timer modulus

Table A-5. Jumper Connector Functions (E5-E8)

Jumper Pins	Channel Atten. Address (E5)	Bus Priority In (E6)	Bus Req. (E7)	Interrupt Level to Main CPU (E8)	Used By Board
1-2	CA7	*BPN7/A25	BRQ7	N/A	
3-4	CA6	*BPN6/A24	BRQ6	INT6	
5-6	CA5	BPN5	BRQ5	INT5	
7-8	CA4	BPN4	BRQ4	INT4	COMM 3
9-10	CA3	BPN3	BRQ3	INT3	COMM 2
11-12	CA2	BPN2	BRQ2	INT2	COMM 1
13-14	CA1	BPN1	BRQ1	INT1	COMM 0
15-16	CA0	BPN0	BRQ0	INT0	

* In systems that support more than 16M bytes of main memory, BPN7 and BPN6 are used for additional system address lines A25 and A24 respectively. When the multidrop communications board is installed in these systems, jumpers must be installed at connector E6 pins 1-2 and 3-4 in addition to the normal BPN jumper setting.



BOARD 0 MEMORY SIZE	BOARD 1 MEMORY SIZE
BOARD 0= 2MB E1 ON; E2 ON	BOARD 1= 2MB* E7 ON; E8 ON
BOARD 0= 4MB E1 ON; E2 OFF	BOARD 1= 4MB E7 OFF; E8 ON
BOARD 0= 8MB E1 OFF; E2 ON	BOARD 1= 8MB E7 ON; E8 OFF

*OR NO SECOND BOARD

ON= JUMPER INSTALLED
OFF= JUMPER NOT INSTALLED

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Figure A-5. Jumpers For Multidrop Communications Boards (Factory Setting)

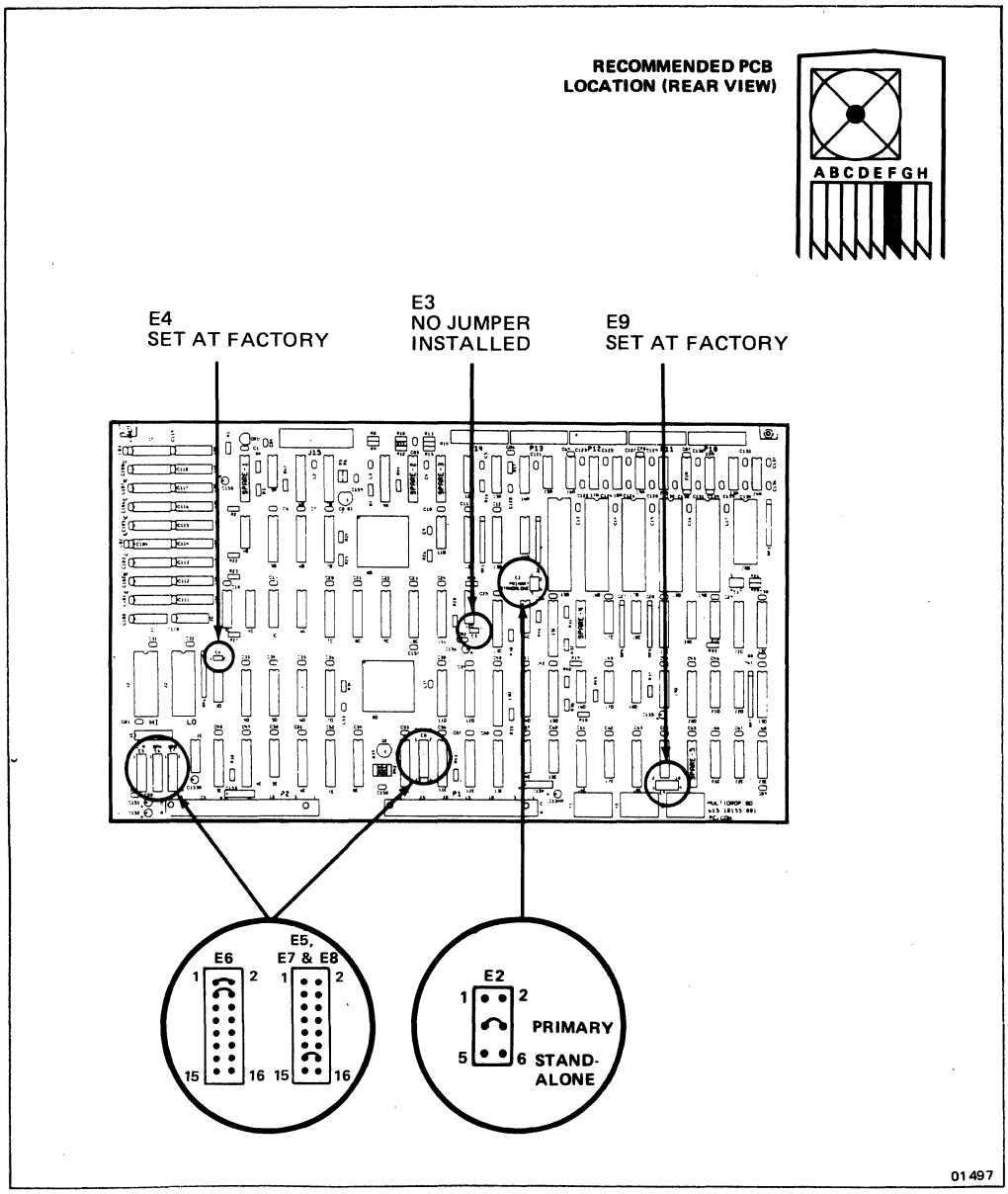

Figure A-6. Jumpers For Multidrop As Primary Communications Board (COMM 0)

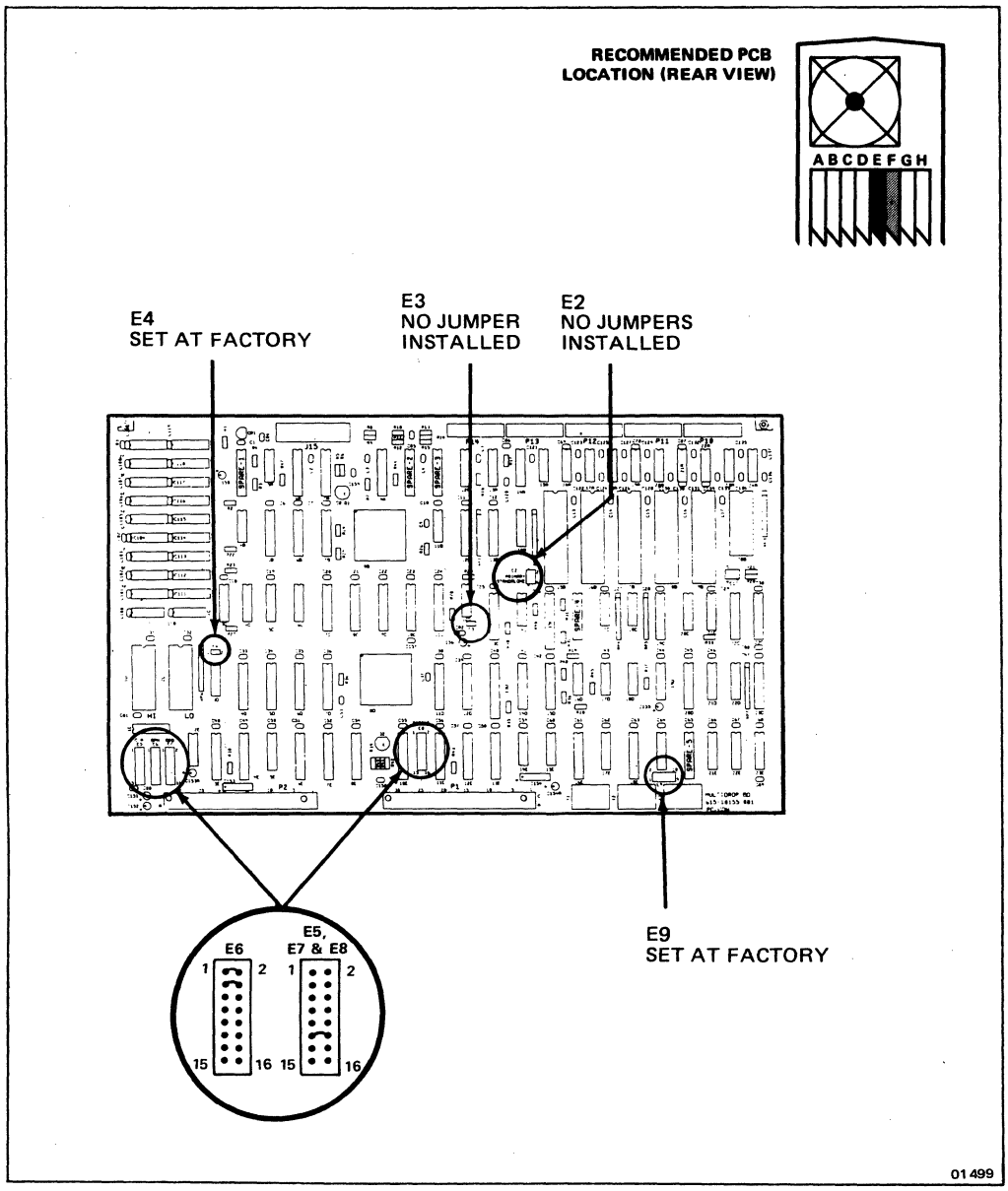

Figure A-7. Jumpers For Multidrop As Second Communications Board (COMM 1)

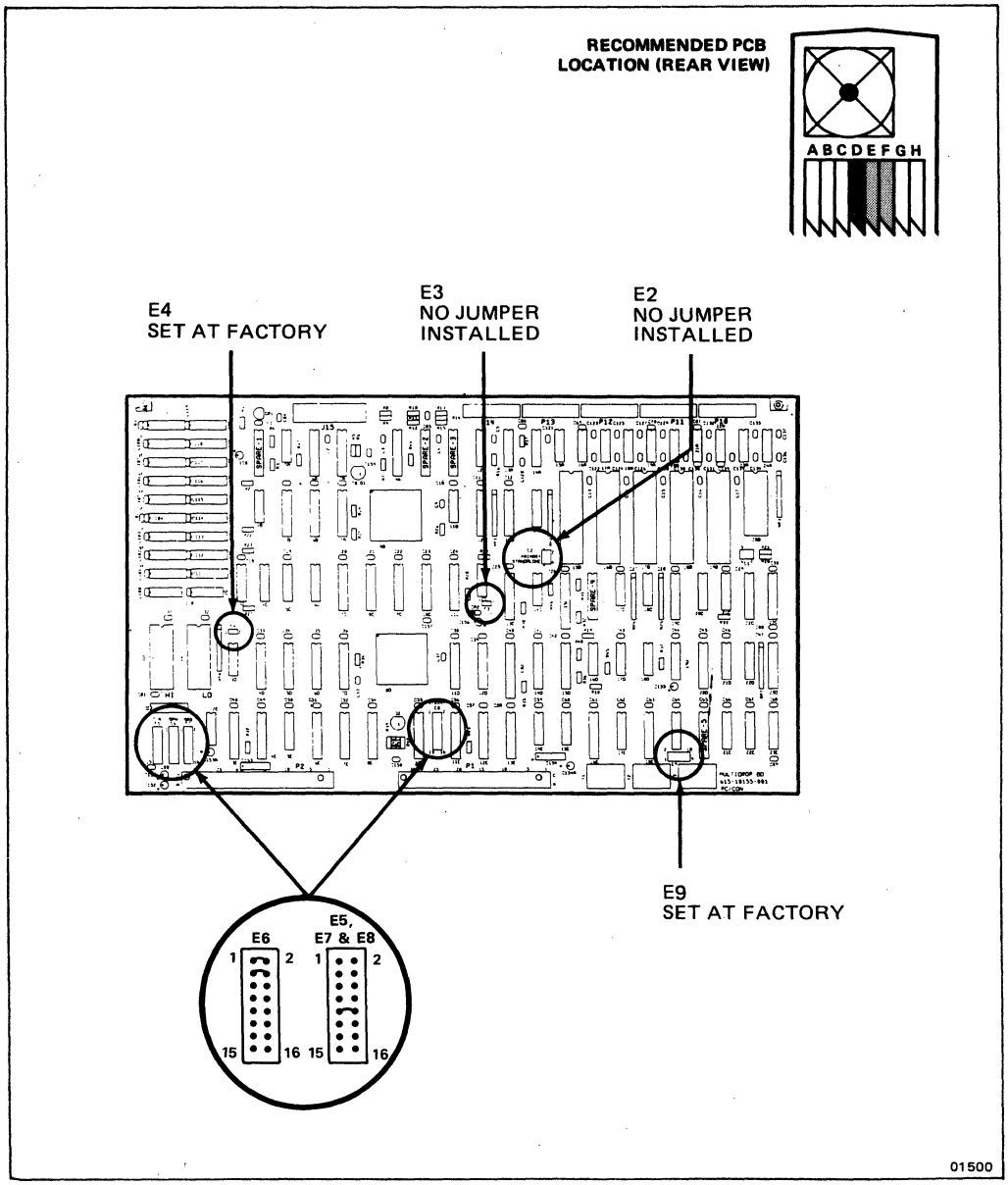

Figure A-8. Jumpers For Multidrop As Third Communications Board (COMM 2)

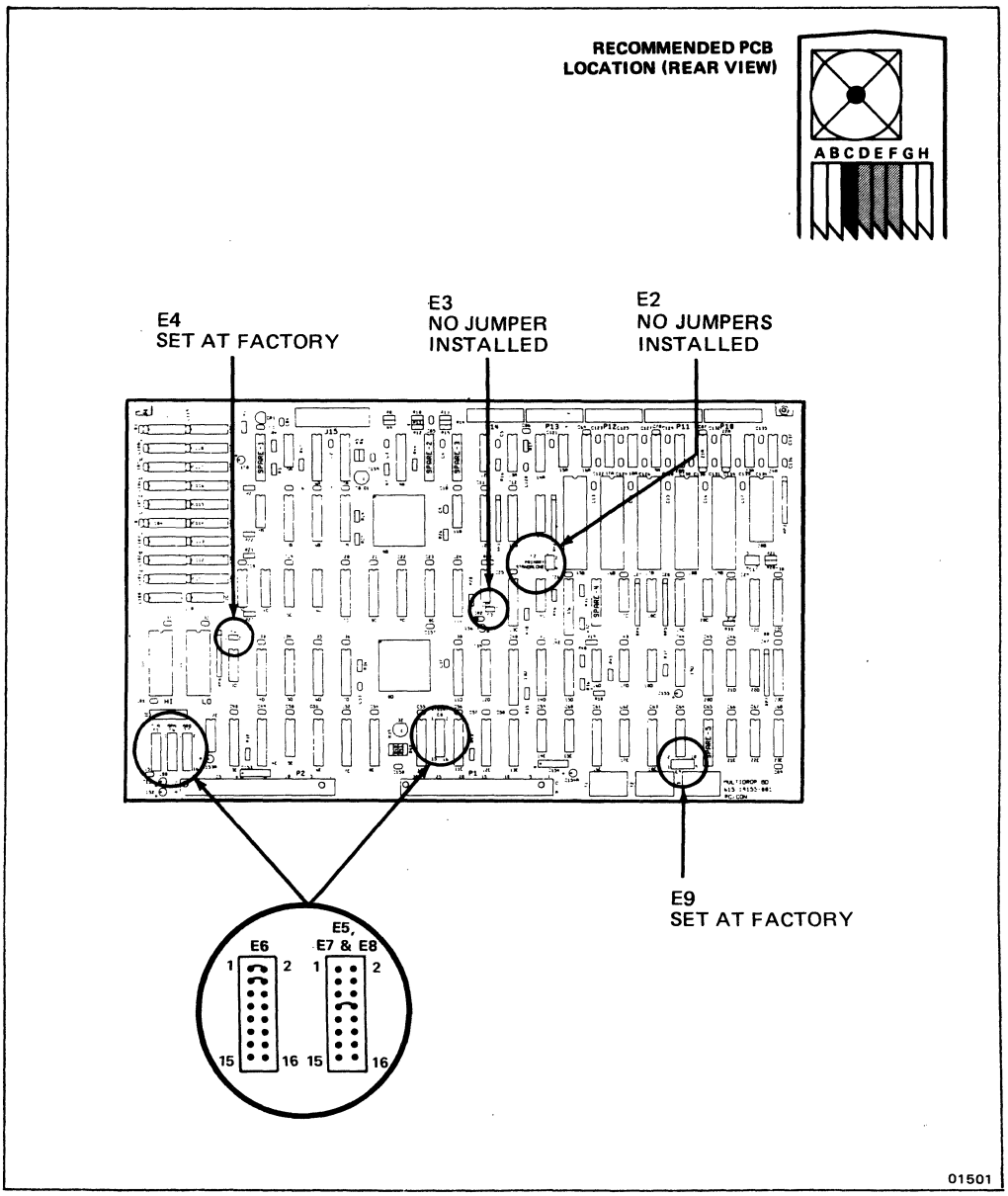

Figure A-9. Jumpers For Multidrop As Fourth Communications Board (COMM 3)

SIO Communications Board Jumpers

The SIO (serial input/output) communications board has eight jumper connectors that are used to select the options described in Table A-6. Figures A-10 through A-14 illustrate the proper jumper connections and recommended slot locations for primary and secondary SIO communications boards.

Table A-6. SIO Board Jumper Descriptions

Connector Designation	Description
E1	General-purpose input port. Jumpered only on the master (0) communications board. Not jumpered on any other communications boards installed in the Series 2000 system
E2	Selects the size of PROMs installed (2732, 2764, or 27128). 2764 PROMs are normally installed
E3	AACK (Advanced Acknowledge). Enables the advanced acknowledge signal from system memory (reduces wait states). Also used for local reset (testing only). Normally jumpered for enabling AACK
E4	BPRN (Bus Priority Input). Used to determine the arbitration priority when the communications board(s) wish to access the system bus
E5	BPRO (Bus Priority Output). See BPRN
E6	CHANATTN (Channel Attention). Selects the port number that the SIO communications board responds to for channel attention signals generated on the system bus
E7	INT. Selects the bus interrupt vector level that the SIO communications board generates
E8	LARGE*. Must be jumpered if 256K dynamic RAMs are installed

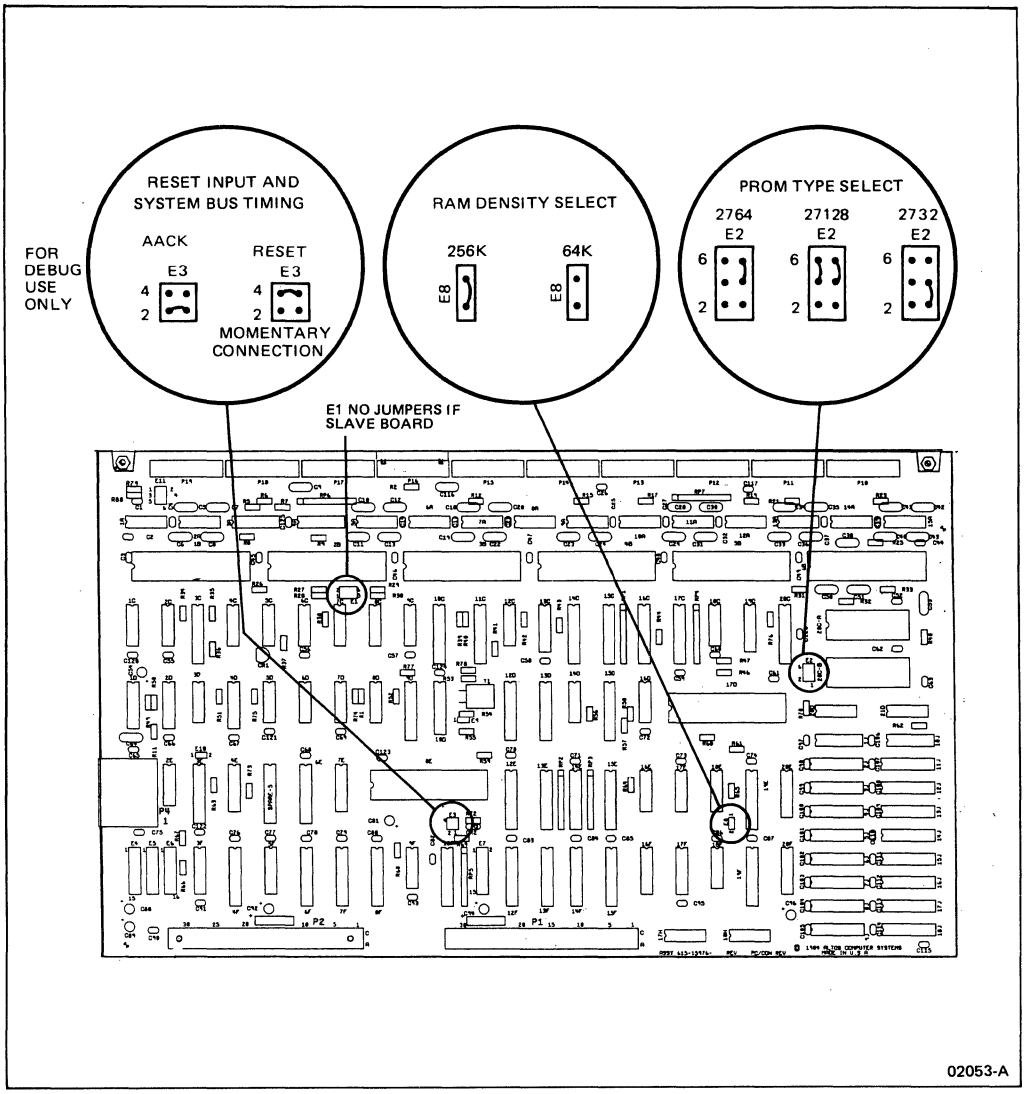

Figure A-10. Jumpers For SIO Communications Boards (Factory Setting)

Figures A-12 through A-14 illustrate the jumper locations and settings for one primary SIO communications board (COMM 0) and three secondary SIO communications boards (COMM 1, 2, and 3). Jumper **E1** is installed only on the primary SIO board.

If there is more than one communications board, set jumpers **E4** through **E7** to indicate COMM 0 (primary), COMM 1, COMM 2, or COMM 3. The settings are shown in Figures A-11 through A-14.

Refer to the **Recommended Board Location** illustrations in Figures A-12 through A-14 and the "Plug-In Printed Circuit Board Locations" discussion in **System Description** - Chapter 1 to determine the proper SIO communications board locations. Installing the boards in the recommended slots makes it easier to troubleshoot and upgrade the system.

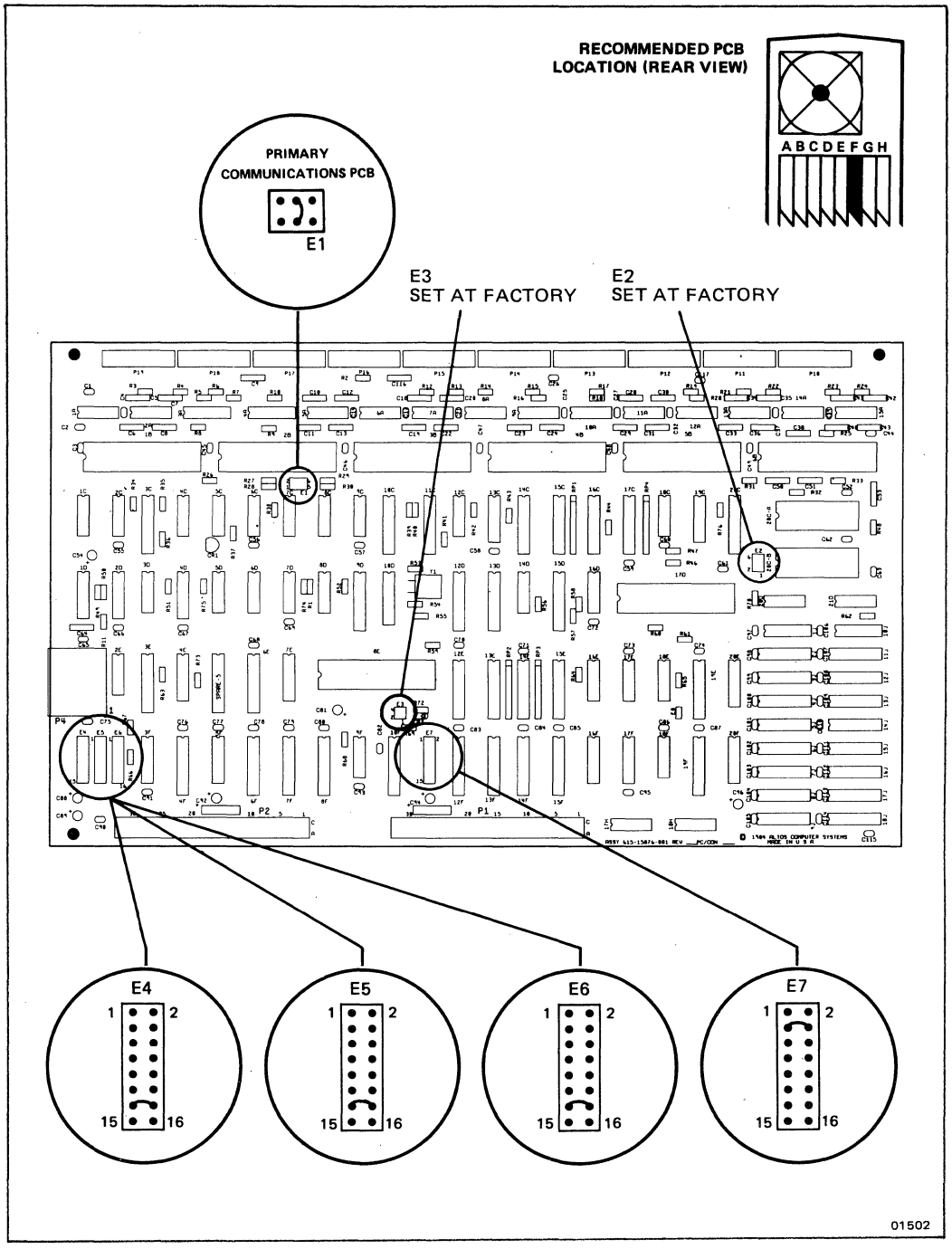

Figure A-11. Jumpers For SIO As Primary Communications Board (COMM 0)

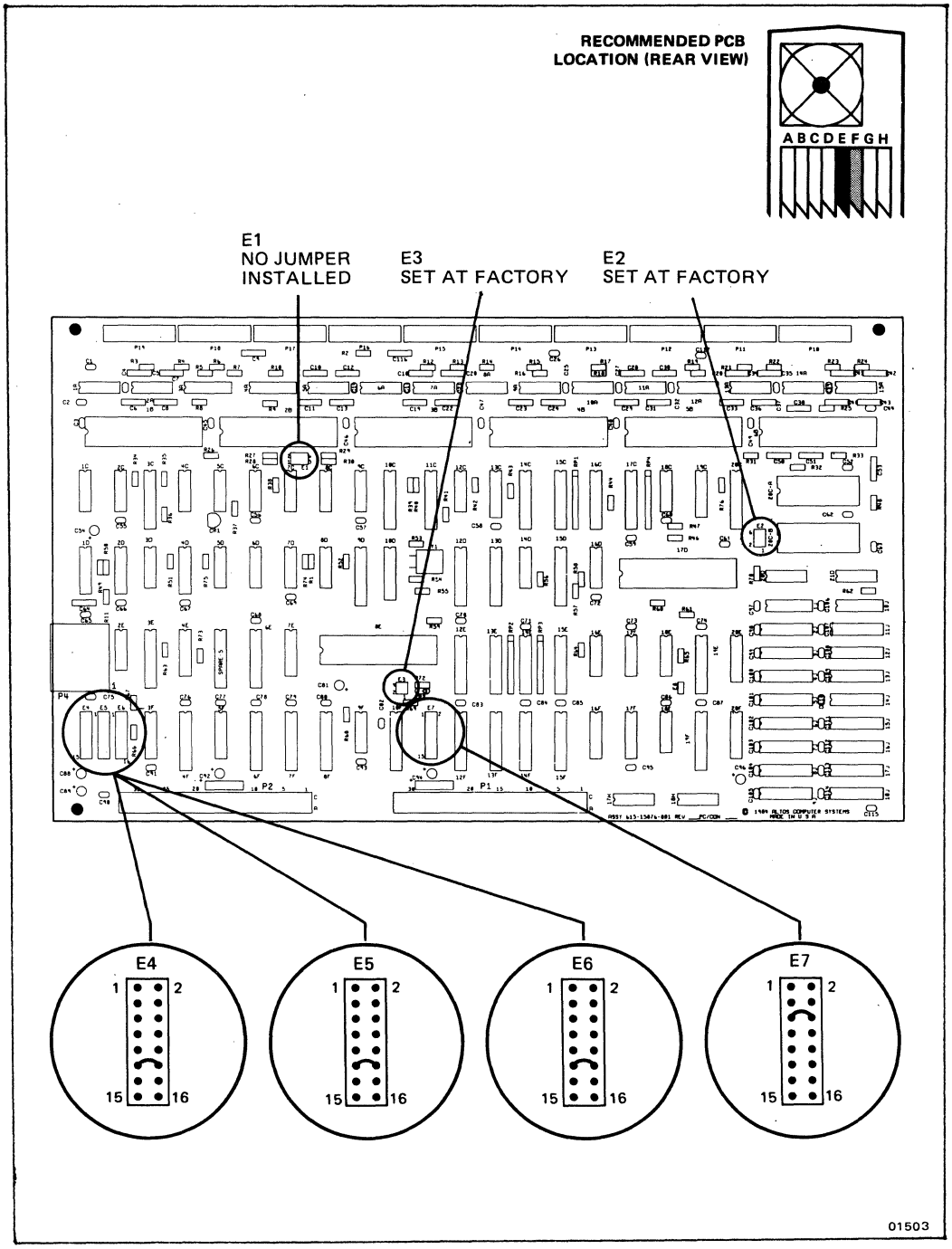

Figure A-12. Jumpers For SIO As Second Communications Board (COMM 1)

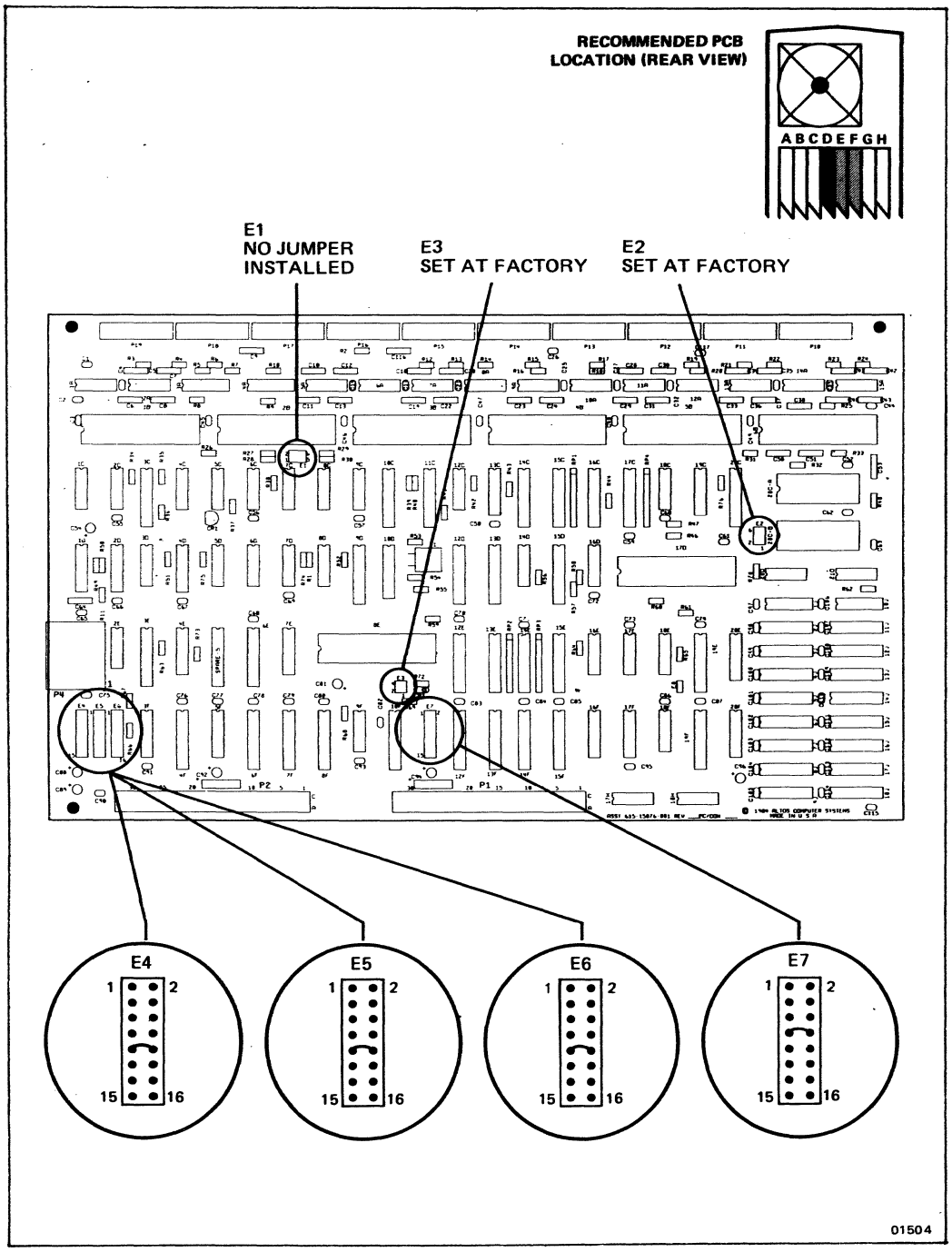

Figure A-13. Jumpers For SIO As Third Communications Board (COMM 2)

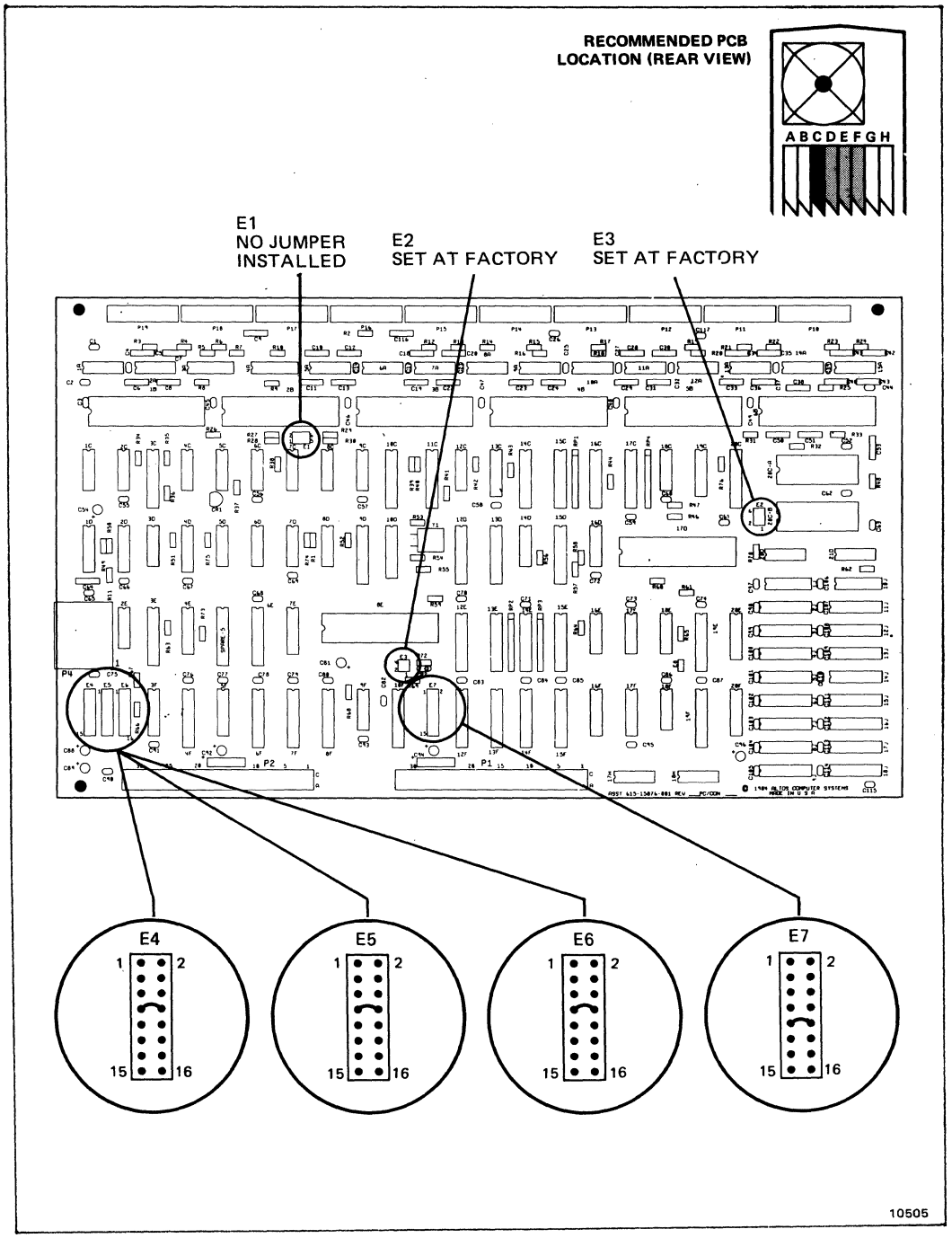

Figure A-14. Jumpers For SIO As Fourth Communications Board (COMM 3)

CPU BOARD JUMPERS

The CPU board has thirteen jumper connectors designated E1 through E13. These jumpers are properly installed at the factory as described in Table A-7 and should not be changed.

Table A-7. Jumper Descriptions

Connector Designation	Description
E1	Real-time clock battery testability (pins 1 and 2 jumpered)
E2	Enables tag address bit 0 for 4K byte tag RAM, 4 byte blocks (pins 2 and 4 jumpered). Disables tag address bit 0 for 2K byte tag RAM, 8 byte blocks (pins 3 and 4 jumpered)
E3	Enables UPS sensing for Altos UPS (pins 1 and 2, and 5 and 6 jumpered). Enables UPS sensing for Topaz UPS (pins 3 and 4 jumpered)
E4	Enables the highest priority master to access the bus when the BPN (bus priority in) signal is the same level as the BRQ (bus request) signal. Single CPU board (pins 5 and 6 jumpered); two CPU boards (pins 5 and 6, and 3 and 4 jumpered); three CPU boards (pins 5 and 6, 3 and 4, and 1 and 2 jumpered)
E5	Enables the highest priority master to access the bus when the BRQ (bus request) signal is the same level as the BPN (bus priority in) signal. Jumpered the same as E4.
E6	Enables the 64 MHz oscillator (2C) to drive 387CLK2 on the 80387 numerical processor (not jumpered for 16 MHz 80386 CPU)
E7	Status bit. Jumper installed if the CPU is running at 20 MHz (pins 1 and 2 jumpered); no jumper installed at 16 MHz

Table A-7. Jumper Descriptions (Cont.)

Connector Designation	Description
E8	Enables bit 2 of the input port to continue the power-up diagnostic tests (no jumper installed). Disables bit 2 to loop on errors for power-up diagnostics (pins 1 and 2 jumpered)
E9	Releases the bus after the address enable (AEN*) signal goes true (pins 1 and 2 jumpered). Releases the bus when another bus master requests it (pins 3 and 4 jumpered)
E10	Enables the cache RAM to fill in 8 byte blocks (pins 1 and 2 jumpered) or in 4 byte blocks (no jumper installed)
E11	Tests the 19.6608 MHz oscillator (pins 1 and 2 jumpered)
E12	Asserts system address bit 2 to enable the cache RAM to fill in 4 byte blocks (pins 1 and 2 jumpered)
E13	Asserts system address bit 2 to enable the cache RAM to fill in 8 byte blocks (pins 1 and 2 jumpered)

Figure A-15 shows the default (shipping) jumper settings for the CPU board.

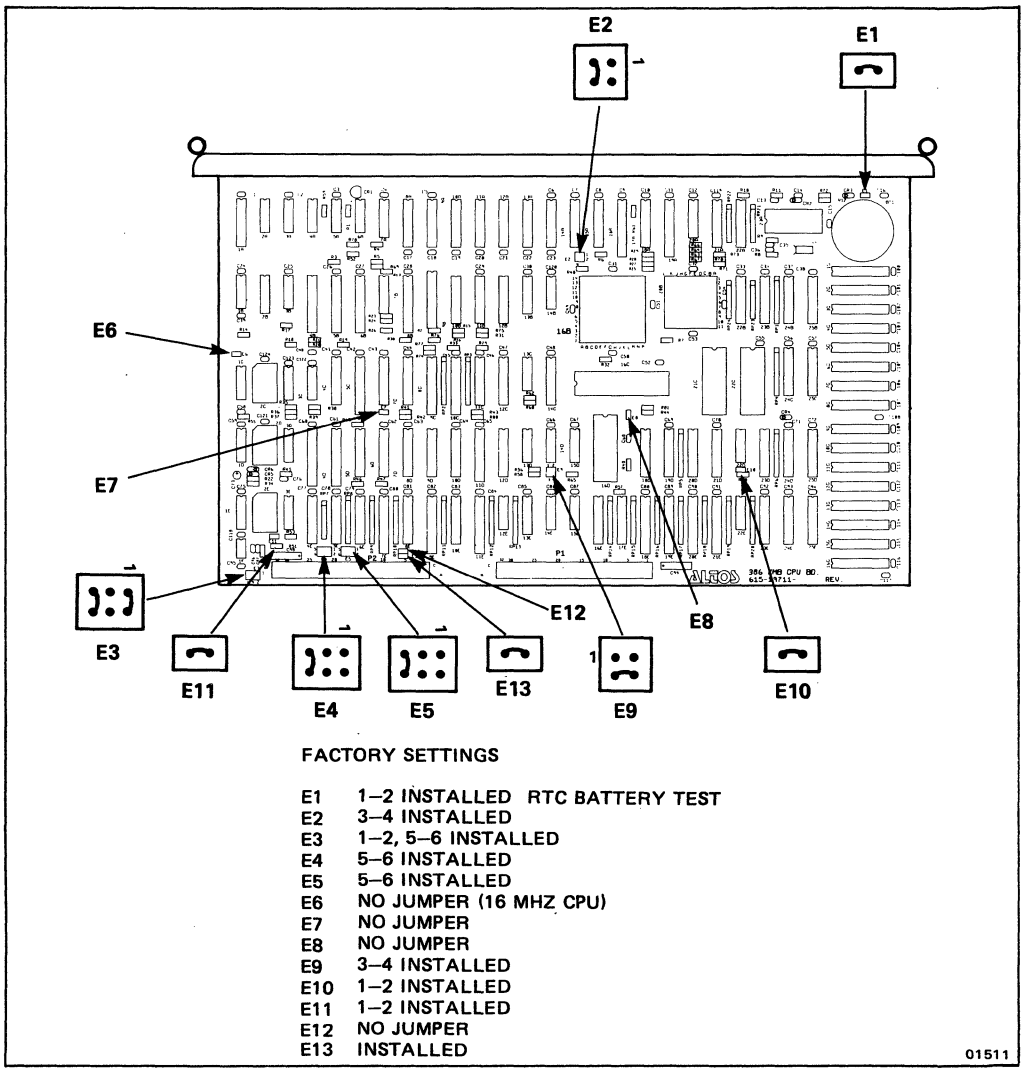

Figure A-15. Default Jumper Settings For the CPU Board

TERMINAL CLUSTER UNIT SWITCHES

The multidrop communications board supports up to 30 RS-422 devices connected to each multidrop interconnect line. Each RS-422 device must be assigned a station identification address by setting the dual-in-line package (DIP) switches located on the TCU.

Before setting the station address switches, there are some conditions that affect the proper operation of the TCU-8:

- your operating system determines the actual number of ports that can be supported by your particular system. Refer to the operating system installation manual for your computer system to determine the number of ports that the operating system will support

- when setting the addresses for any device on the multidrop line, be careful to ensure that the addresses are unique, and there are no address duplications or overlaps

- the TCU-8 responds to eight addresses regardless of how many RS-232 devices are attached to the TCU

- the TCU station identification switches are only read once at the time that the TCU power is turned on. If the switches are changed while the TCU power is on, the TCU power must be turned off then on again before the new switch settings will take effect

Station Address Selection

Refer to Table A-8 for the possible station identification switch settings for the TCU-8. See Figure A-16 for an example of the TCU-8 station identification switch and port address relationships and Figure A-17 for the station address bit assignments beginning with the most significant bit (MSB).

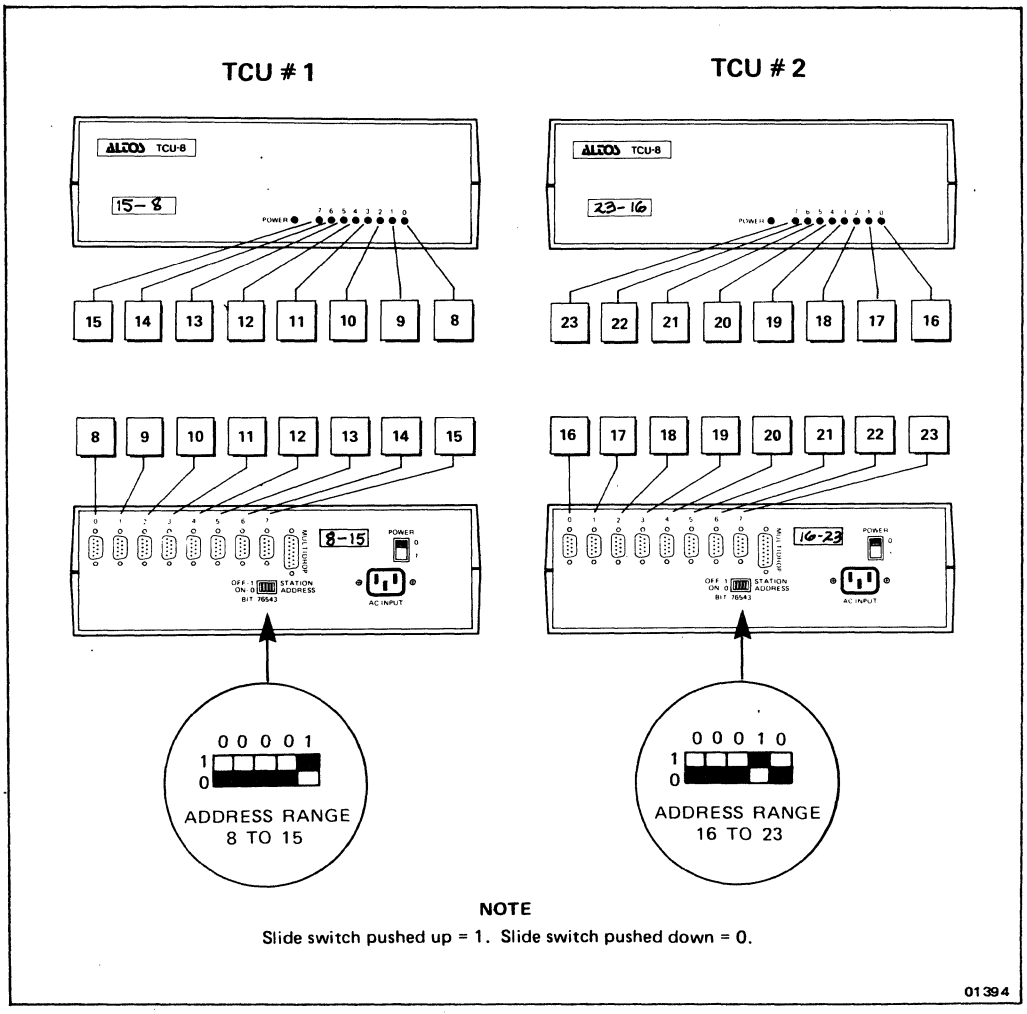

Figure A-16. Station Identification Switch to Port Address Relationship

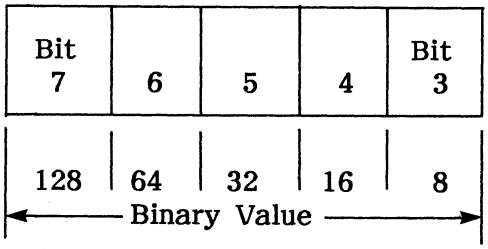

Figure A-17. Station Address Switch Bit Assignments

Table A-8 shows the switch settings for a specific range of addresses. A "1" means the up (off) switch position; a "0" means the down (on) switch position.

Table A-8. Station Identification Switch Settings

Station Addresses	Switch Setting 7 6 5 4 3	Station Addresses	Switch Setting 7 6 5 4 3
0 - 7	**Do not use**	128 - 135	1 0 0 0 0
8 - 15	0 0 0 0 1	136 - 143	1 0 0 0 1
16 - 23	0 0 0 1 0	144 - 151	1 0 0 1 0
24 - 31	0 0 0 1 1	152 - 159	1 0 0 1 1
32 - 39	0 0 1 0 0	160 - 167	1 0 1 0 0
40 - 47	0 0 1 0 1	168 - 175	1 0 1 0 1
48 - 55	0 0 1 1 0	176 - 183	1 0 1 1 0
56 - 63	0 0 1 1 1	184 - 191	1 0 1 1 1
64 - 71	0 1 0 0 0	192 - 199	1 1 0 0 0
72 - 79	0 1 0 0 1	200 - 207	1 1 0 0 1
80 - 87	0 1 0 1 0	208 - 215	1 1 0 1 0
88 - 95	0 1 0 1 1	216 - 223	1 1 0 1 1
96 - 103	0 1 1 0 0	224 - 231	1 1 1 0 0
104 - 111	0 1 1 0 1	232 - 239	1 1 1 0 1
112 - 119	0 1 1 1 0	240 - 247	1 1 1 1 0
120 - 127	0 1 1 1 1	248 - 255	**Do not use**

Status Lights

The TCU-8 has status (LED) lights that provide status indications for the multidrop system. Refer to the *Series 2000 Owner's Guide* for additional information.

Table A-9 describes how to use the TCU status lights to determine the status of the multidrop system.

Table A-9. Using the Status Lights

Light Condition	Probable Cause	Remedy
One or more lights flashing:		
1 long; 1 short	Power-up test failure, ROM checksum	Return to factory
1 long; 2 short	Power-up test failure, UART	Return to factory
1 long; 3 short	Power-up test failure, RUPI	Return to factory
1 long; 4 short	Attempt to use an illegal address (0 or 255)	Check and/or change the illegal TCU address (all 0's or all 1's)
Solid off	OFF-LINE -- no polling is taking place; communication between TCU and host is not occurring	Normal when port is disabled by operating system -- if enabled, check cable from *MDC to TCU; check port parameters

Table A-9. Using the Status Lights (Cont.)

Light Condition	Probable Cause	Remedy
Medium steady blink (on 3/8 second, off 1/8 second)	NEGLECTED -- not polled for 2 - 4 seconds; will go off-line if no action is taken in 2 minutes (you can override this in the operating system)	If enabled, check cable from *MDC to TCU; check port parameters
Solid on	ON-LINE -- polling is taking place; TCU is communicating with *MDC; port is enabled	Normal TCU condition when active
Fast steady blink (on 1/8 second, off 1/8 second)	DUPLICATE ADDRESS ERROR -- two devices with same address	Check and change address

* Multidrop communications board

Normally, when the TCU-8 is powered on, all the status lights go on for approximately two seconds. Then, the green power light should remain on while the other lights should be on, off, or blinking as described in Table A-9.

Appendix B
Utilities

(BLANK)

INTRODUCTION

This appendix includes procedures for using the utility programs available on the Field Diagnostics Executive (FDX) disk available as part of the maintenance package from Altos Customer Support. The utility programs enable you to:

- prepare a floppy disk for use
- copy a floppy disk
- display the bad sectors on the hard disk
- flag additional bad sectors on the hard disk
- remove bad sector flags on the hard disk
- rebuild drive configuration and bad sector information
- reformat the hard disk
- set the real time clock

Before you can use the FDX utility programs, boot from the FDX disk as described in the following procedure. The FDX utilities are available only from the system console terminal.

BOOTING THE FDX DISK

Perform the following procedure to boot the FDX disk:

1. Turn on the system power. If the system power is on, turn the reset key to RESET and back to RUN.

2. Press the **Space Bar** when you see the prompt:

```
Press any key to interrupt autoboot
```

The following menu appears:

```
1) Boot from hard disk
2) Boot from floppy disk
3) Enter the main CPU monitor
4) Enter the main MDC monitor
5) Boot from streaming tape
```

3. Insert the FDX disk into the floppy disk drive.

4. Type **2** to select the floppy disk boot. A message similar to the following appears:

```
Booting from floppy (low speed)
Loading, please wait
```

5. Wait for the FDX Main Menu to appear:

```
FIELD DIAGNOSTIC EXECUTIVE (FDX) VERSION 1.XX

Main Menu:

        R:  Run system confidence tests
        U:  Utility programs
        S:  Display test summary
        F:  Go to Field Service Menu
        X:  Exit Field Diagnostic Executive (FDX)


*** Enter command and press <Retn>:
```

If the Main Menu does not appear, repeat steps 3 and 4.

6. When the Main Menu appears, press **f** and **Retn**. The following Field Diagnostic Executive Menu will appear:

```
Field Diagnostic Executive Menu:

      b (brief)      Brief description of all tests
      c (clear)      Clear pass count, error count, and history
      d (disable)    Disable test
      e (enable)     Enable test
      h (halt)       Halt on error
      l (loop)       Loop on command line
      m (menu)       Menu level selection
      p (parameter)  Change parameters
      r (report)     Display error history
      s (summary)    Display error summary
      t (test)       Execute test (s)
      u (utility)    Call utility programs
      ? (help)       Display this menu
      x (exit)       Exit to Main Menu
      z (debugger)   Enter Debugger

      ***Enter Command and Press <Retn>
```

7. Type **u** and **Retn** to select the utility programs. The following Utility Menu appears:

```
Utility Menu

      Utility #    Utility Description

      1            Floppy Format
      2            Floppy Copy
      3            Display Bad Sector/Configuration Tables
      4            Flag Hard Disk Bad Sectors
      5            Rebuild Hard Disk Tables
      6            Reformat Hard Disk
      7            Real Time Clock Utilities
      8            Return to Previous Menu

      Enter Selection and press <Retn>
```

CAUTION

The utilities in the Field Diagnostic Executive Menu contain several important utilities that should be used by factory-trained service personnel. Uninformed use of these utilities can destroy all data on the hard disk, and render the hard disk unusable.

8. Select the utility you want by typing in the program number. Then find the procedure for your selection in the remainder of this appendix.

NOTE

If you need to stop a program before it completes, press the Esc key. Pressing Esc cancels the operation and pressing any key returns you to the Main Menu.

FLOPPY FORMAT

The floppy drive operates at two speeds: high speed and low speed. When you use the FDX Floppy Format and Floppy Copy utilities, the display asks whether you want to format at high or low speed, and adjusts the speed accordingly.

Use high speed to read and write to floppy disks created at high speed. Use low speed to read and write to disks created at low speed (e.g., on earlier Altos systems, and on IBM PC and XT computers). Refer to your software documentation for information on accessing floppy disks created on other floppy drives.

NOTE

Make sure you use certified, high-density, double-sided, soft-sectored, 96 tpi (tracks per inch) disks if you plan to format a disk at high speed.

Always format a floppy before trying to use it under the operating system. If you try to use the operating system to access information on an unformatted disk, you will receive an error message similar to:

```
dev_stat [0/1/2/3] xxh xh xh xxxxh general error
```

CAUTION

Formatting a floppy disk erases all data on the disk. Do not format a disk that contains any valuable data.

1. Press **1** and Retn. The screen displays:

```
Floppy Format                Please wait...

Enter the floppy speed or <Esc> to exit:

(A) Low Speed       (B) High Speed

Enter:
```

If you have the optional dual-speed floppy, you can format the disk at high or low speed.

2. Enter the floppy speed. The following prompt asks if you want each track to be verified:

```
Do you want track verification?  (y/n)
```

3. Enter **y** (yes) to verify each track as it is formatted to assure that the formatting process is successful.

   Track verification increases the execution time of the formatting process to approximately three minutes for each disk. Without track verification, the process takes approximately one minute. After responding to the track verification prompt, the screen displays:

```
Insert diskette to be formatted and press "Y"
```

4. Remove the disk from the drive and insert the disk to be formatted. Then press **y**.

   As the disk is formatting, the screen displays the number of each cylinder. If you select track verification, the screen also displays the number of each cylinder as it is verified. After formatting is completed, the screen displays:

```
          Format completed.

Do you wish to run this program again? (y or n)
```

5. Select **y** (yes) and press Retn if you want to format additional floppy disks.

   To return to the Utility Menu, enter **n**, press Retn, and follow the instructions.

FLOPPY COPY

You do not have to format a disk before using the Floppy Copy utility. The display asks you to select which speed you want to use. You can use high speed to copy a high-speed disk to an unformatted certified high-speed disk. You can use low speed to copy one standard disk to another standard disk.

You can also use low speed to copy information from a low-speed disk onto a high-speed disk, but the program automatically formats the destination disk at low-speed before copying the information.

If you select high speed and try to copy information from a high-speed disk onto a low-speed destination disk, you will receive an error message. If you have to transfer information from a high-speed disk to a low-speed disk, use the operating system software to copy the disk to the hard disk. Then transfer it onto the low-speed disk.

NOTE

To copy a high-speed disk, you must use a high-speed certified disk as the destination disk (the disk you copy to). Standard disks do not work correctly when used at high speed.

Return to the Utility Menu and perform the following procedure to copy a disk:

1. Type **2** and press Retn to select Floppy Copy from the Utility Menu.

2. Wait for the screen to display:

```
Floppy Copy                    Please wait...
```

3. Wait for the following display to appear:

```
Enter the floppy drive speed or ESC to exit:

   (A) Low Speed          (B) High Speed


Enter:
```

4. If you want to copy information from a low-speed disk to another low-speed disk, answer **A** and press Retn. If you want to copy information from a high-speed disk to another formatted high-speed disk, answer **B** and press Retn. The screen displays:

```
Insert diskette to be copied from and press 'y'
```

5. Insert the disk to be copied from. Type **y** and Retn. The screen displays:

```
*** Reading cyl:  nn
```

6. Wait for the first read cycle to complete. The screen displays:

```
Insert diskette to be copied to and press 'y'
```

7. Insert the disk to be copied to. Type **y** and Retn. The screen displays:

```
*** Writing cyl:  nn
```

When the copy is complete, the screen displays:

```
Copy completed.  Do you wish to run this program again?  (y/n)
```

8. Type **y** and **Retn** to continue copying disk until you have no more disks to copy. To exit from Floppy Copy, type **n**. The screen displays:

```
Floppy Copy.....................Executed

Press any key to return to the Utility Menu.
```

9. Press any key, such as the **Space Bar** to return to the Utility Menu.

10. Type **8** and **Retn** to exit from the Utility Menu.

WORKING WITH HARD DISK BAD SECTORS

Terminology

The remaining utilities in the Utility Menu deal with the hard disk drive bad sectors. The following information is intended to help explain some of the hard-disk terminology relating to these utilities.

The hard disk stores data in hundreds of circular tracks, which are further divided into sectors. Hundreds of thousands of individual sector areas are available on each hard disk. Figure B-1 shows the differences between hard-disk sectors, cylinders, and heads.

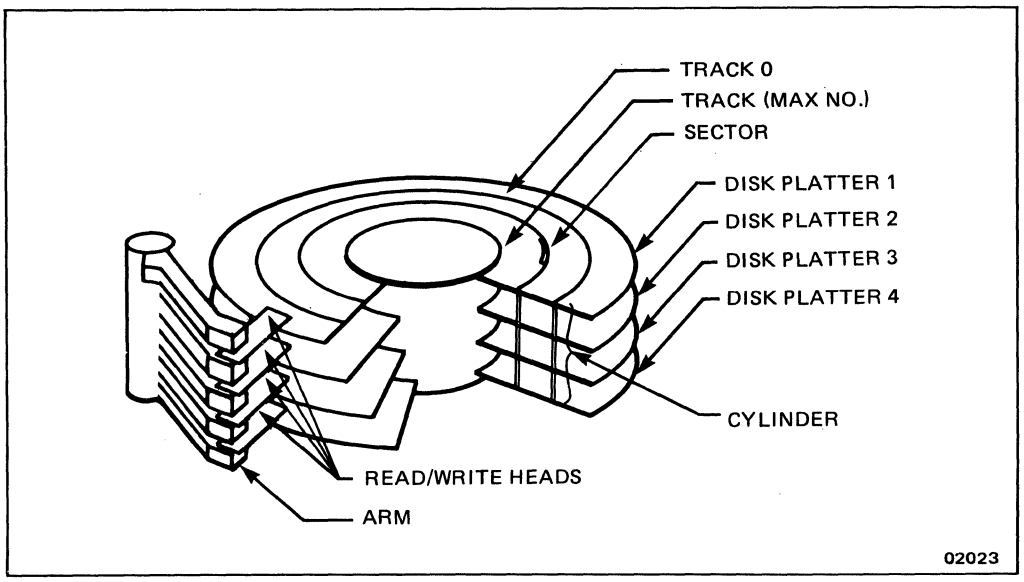

Figure B-1. Hard-Disk Terminology

Occasionally a sector develops a flaw in the magnetic media. These bad (flawed) sectors do not noticeably reduce hard disk storage, but the system needs to identify the bad sectors, so that no data is stored on them.

Each hard disk drive is carefully tested at the factory and any bad sectors are flagged before shipment. A hard copy printout of the flaw list is included for each hard disk drive. An identical list is also stored on track 0 of each hard disk. If there is more than one hard disk drive, match the lists with the correct drives.

To do this, compare the serial number on the printout with the serial number written on the round label in the front of the drive. (Remove the front panel to check the round labels -- refer to **Maintenance** - Chapter 6 for removal and replacement procedures.)

When you use the utility programs to display the current list of bad sectors, the program gets the list from track 0. Use the Scan Hard Disk for Bad Sectors utility to scan the disk and list any bad sectors that do not correspond to the current list. Make sure you use the Flag Bad Sector utility to flag any unflagged bad sectors immediately.

At some time, you may receive a message from your operating system software that a new bad sector has been found. The message is similar to:

```
hard disk error drv x cyl xxxx hd x sec xx, or
marginal sector drv x cyl xxxx hd x sec xx
```

Make sure you write down the drive (drv), cylinder (cyl), head (hd), and sector (sec) numbers accurately. Then use the Flag Bad Sector utility to flag the new bad sector. The flag bad sector utility allows you to update the track 0 information.

Make a copy of the flaw list printout and keep it. If new bad sectors occur while you use the system, update the list with the drive, cylinder, head, and sector locations. You may need the entire list if the information on track 0 is ever destroyed.

Determining the Drive Number

Before you can use the following utilities, you need to understand how the hard disk drives are numbered in your system. The first drive is installed in the bottom drive slot, and is called drive 0. The second drive, if you have one, is installed in the middle slot and called drive 1.

The third drive, if present, is installed in the top slot and is numbered drive 2. When the following hard-disk utility programs ask you to specify which drive(s) you want to test, enter a **0, 1,** or **2.**

DISPLAY BAD SECTOR/CONFIGURATION TABLE

The Display Bad Sector/Configuration Table utility program from the Utility Menu allows you to view technical information about the hard disk(s). This utility lists the number of cylinders, heads, sectors, sector size, track skew, sector interleave, manufacturer, size in megabytes, and precompensation information.

The bad sector table information is contained in two locations, track 0 and the maximum outermost track on the hard disk. Sectors 0, 6 and 7 contain a copy of the main drive configuration table and the bad sector table on Track 0. A duplicate copy of the same information resides on the maximum track and maximum head in the first usable three sectors. This duplication of the drive configuration and bad sector information on two different locations on the hard drive reduces the likelihood of losing the drive configuration information and bad sector information.

Note the distinction between "added" and "original" flags. "Original" flagged bad sectors were flagged at a format and flag station at the factory while "added" flags were found during the production process.

Perform the following procedure to use this utility:

1. Type **3** and press **Retn** to select the Display Bad Sector/Configuration Table utility. The following screen appears:

```
Enter the hard drive from the list or press <Esc> to exit.
(0) Drive  0
(1) Drive  1
(2) Drive  2

Enter -
```

2. Type a **0, 1,** or **2** to indicate which drive you are checking. For example, type **0** for a one-drive system. Information similar to the following appears:

```
Drive 0 is a Micropolis with 170MB capacity with:
1024 cylinders per drive.
8 heads per drive.
35 sectors per track.
Track skew of 4.

Would you like to see the bad sector list ? [y/n]
```

3. Type **y** and Retn to see the list; type **n** and Retn to return to the Utility Menu. If you type **y**, press any key when you see the message:

```
Press any key to continue
```

When the last screen displays, you will see information similar to the following:

```
Bad Sector Table for Drive #0
Line 0001 Drive X Cylinder XXXX Head XX Sector XX is an added flag.
Line 0002 Drive X Cylinder XXXX Head XX Sector XX is an added flag.
Line 0003 Drive X Cylinder XXXX Head XX Sector XX is an original flag.
Line 0004 Drive X Cylinder XXXX Head XX Sector XX is an original flag.
Line 0005 Drive X Cylinder XXXX Head XX Sector XX is an original flag.

Display Bad Sector Configuration Table.....Executed

Press any key to return to the Utility Menu.
```

NOTE

Due to the large capacity of the hard disks, it is not unusual to have a bad sector list with one hundred or more entries.

4. Press any key to go back to the Utility Menu.

FLAG HARD DISK BAD SECTORS

CAUTION

If there are any files on the hard disk, make a backup copy of the files before you continue. Setting a bad sector flag blocks off any information in the sector you flag.

There are two occasions when you may need to flag hard disk bad sectors:

1. If you need to mark (flag) new bad sectors which occur on the hard disk during operation. (A new bad sector is a disk flaw area that develops after the original list was created at the factory.) This may never occur, but if it does you will receive an operating system message similar to:

```
hard disk error drv x cyl xxxx hd x sec xx
```

2. If you experience a serious problem with the hard disk which requires recalibrating the drive. (Recalibration involves reformatting track 0 on the hard disk.)

Drive Serial Number

A hard copy printout of the bad sectors is included with each hard disk drive. Each drive has a sticker with a serial number (to see

the serial numbers you must remove the front panel as described in Chapter 4). The flaw list printout has the same serial number.

Entry Mode

Some hard disk suppliers identify sectors using the number of bytes offset from index, while others use physical sector numbers. The FDX software lets you enter sector information using any of these methods.

NOTE

You must reinstall the operating system software if you flag additional hard disk bad sectors. Refer to your operating system manual for details.

Perform the following procedure to flag a hard disk bad sector:

1. Type **4** to select the **Flag Hard Disk Bad Sectors** utility. The following information appears:

```
Enter the hard drive from the list or press <Esc> (X) drive X
Enter -

Flag Menu

(0) Add flags to Bad Sector Table
(1) Delete flags from Bad Sector Table
(2) Save Bad Sector Table to hard disk
(3) Display Bad Sector Table in Memory
(4) Exit from this utility

Enter selection <Retn>
```

2. Enter a **0** to select **Add flags to Bad Sector Table.**

3. Wait for the following display to appear and enter the track, head, sector, and bytecount location of the bad sector.

```
Track (Enter <Retn> to terminate input) -
Head -
Sector -
Bytecount -
```

After you add or delete flags from the Bad Sector Table, you must use option 3 from the Flag Menu to actually save all the entries into the bad sector tables on the hard disk drive. Since the bad sector information is not automatically saved, you can quit and retain the old bad sector table if you make a mistake while entering the bad sector information.

The Micropolis Model 1355, for example, has a bad sector map attached to the top of the drive giving the track, head, and sector location in decimal numbers in bytes from the index. In this mode the utility prompts you for the track, head, and sector of each bad sector. After you have entered the last bad sector, press Retn to exit, and then if you entered all the bad sectors correctly use option 3 to save the bad sector table to hard disk.

NOTE

If you decide that you do not want to flag a bad sector, press Retn. Pressing Retn will take you out of the **Flag Hard Disk Bad Sectors** utility and return you to the Utility Menu without changing the sector information on the hard disk.

4. If you do not wish to enter another sector, press Esc. If you wish to continue flagging bad sectors, press Retn.

5. If you are sure that you want to add this bad sector to the list on cylinder 0, type **2** to select **Save Bad Sector Table to hard disk.** The screen displays:

```
Are you sure? (y/n)?
```

If you are sure, answer **y** (yes). The program will not add the new bad sector to the list unless you take this step!

6. If you do not want to add this the sector to the list on cylinder 0, type **4** to select **Return to Utility Menu.** The screen asks: **Are you sure? (y/n)?.** If you are sure, answer **y.** The program will not add the new bad sector to the list if you answer **y.**

NOTE

If you mistakenly flagged a sector or wish to remove the flag from a sector that has proven to be good, repeat the preceding procedure except type **1** instead of **0** in step 2.

REBUILD HARD DISK TABLES

The Display Bad Sector/Configuration Tables and the Rebuild Hard Disk Tables utilities are provided so that if a hard drive has its drive configuration and bad sector information destroyed, these utilities can be used to rebuild this information.

If the Display Bad Sector/Configuration Table utility showed that a hard disk drive was either missing drive configuration or bad sector information, the Rebuild Hard Disk Tables provide a convenient method for retrieving this missing information.

Perform the following procedure to use this utility:

1. Type **5** and press **Retn** to select **Rebuild Hard Disk Tables.** The following screen will appear:

```
Rebuild Hard Disk Tables

Enter the hard drive from the list or press Esc to exit.
(0) Drive  0
(1) Drive  1
(2) Drive  2

Enter -
```

2. Enter a **0, 1,** or **2** to indicate which hard disk drive you are checking. For example, type **0** for a one-drive system. The screen displays:

After the hard drive is selected, the Rebuild Hard Disk Tables allows you to choose from the following functions:

```
Enter drive to rebuild or ESC to exit.
(X) drive X.
Enter - 0
Enter desired function:
(1) Rebuild Drive Configuration from backup table.
(2) Rebuild Bad Sector from backup table.
(3) Rebuild backup Drive Configuration from main table.
(4) Rebuild backup Bad Sector from main table.
(5) Rebuild drive configuration tables.
(6) Rebuild Bad Sector Tables.
(7) Exit this utility.
Enter -
```

Functions 1 and 2 rebuild the main backup tables from maxtrack. Functions 3 and 4 rebuild the backup drive configuration and bad sector tables from the main tables on track 0. In the event of hard drive crash, use either the main tables or the backup tables

to restore the bad sector or drive configuration information. If the drive configuration or bad sector information on track 0 has been destroyed, use the backup tables on maxtrack (functions 1 and 2).

As mentioned previously, the bad sector table information is contained in two locations: track 0 and the maximum innermost track on the hard drive. Sectors 0, 6, and 7 on track 0 contain a copy of the main drive configuration table and the bad sector table. A duplicate copy of the same information resides on the maximum track and maximum head in the first usable three sectors, which is called maxtrack, and contains the backup tables. The operating system uses the main table to map out the hard drive, and FDX uses the backup tables so that it can distinguish between "added" and "original" bad sectors.

In addition to the drive configuration and bad sector information, the backup tables contain the number of sectors added to the bad sector table. Specifically, the first 27 bytes of the backup table match the main table. Byte 27 locates the sector on maxtrack that the first sector of the backup bad sector resides on. This is done because it is possible for maxtrack itself to have a media defect. Byte 28 locates the second sector of the backup bad sector information.

Finally, byte 29 contains the the number of sectors added to the sector table. These are the "added" bad sectors. Any sector that is not contained on the original manufacturer's Bad Sector Map is considered an "added" flag and is included in this number.

If this fails, functions 5 and 6 erase both track 0 and maxtrack. If you really need to start over (e.g., reenter all the bad sectors from the manufacturer's bad sector list and/or reconfigure the hard drive) use functions 5 and 6 along with the Flag Hard Disk Bad Sector utility. If you select functions 5 or 6, the utility informs you that the prior information at track 0 and maxtrack will be destroyed. For example, if you enter function 6 the following screen will appear:

```
This utility will alter the bad sector table on drive 0111
DO YOU WANT TO CONTINUE (Y/N)?
```

If you answer **y** (yes), the following screen will appear:

```
Initializing bad sector list to zero
Please Use Flag Hard Disk Bad Sector Utility to reflag bad sectors
Rebuild Hard Disk Table.........Executed


Press any key to return to the Utility Menu.
```

REFORMAT HARD DISK

Use the **Reformat Hard Disk** utility to reformat the hard disk.

CAUTION

This utility destroys all data on the hard disk and requires that you back up all files onto tape or floppy disks before you format the hard drive. Once the hard disk has been formatted, the operating system will have to be reinstalled onto the hard disk.

Perform the following procedure to reformat the hard disk:

1. Press **6** and Retn to select the **Reformat Hard Disk** utility. The following display appears:

```
Hard Disk Format
0 - Drive - 0
1 - Drive - 1
2 - Drive - 2

Enter a drive number from the above selection

->
```

2. Enter the number of the drive that you wish to format. The display asks:

```
Would you like to reconfigure the drive information on Drive? y/n
->
```

3. Press **y** (yes). A caution appears:

```
CAUTION - This utility will erase all files on hard drive X!!!.
Formating the entire surface of XXXX drive X
Cylinder = XXXX
```

4. Press **y** again to reformat the hard disk. The program counts sequentially through the cylinders as they are formatted and displays:

```
Formatting Hard Disk Drive 0

Cylinder XXXX

Press any key to return to the utility menu.
```

5. When the hard disk drive has finished formatting all the cylinders, press any key to return to the Utility Menu.

REAL TIME CLOCK UTILITIES

Use the **Real Time Clock Utilities** from the Utility Menu to display the real time clock, set the clock, and write the real time clock non-volatile RAM. Perform the following procedure to use this utility:

1. Type **7** and Retn to select **Real Time Clock Utilities.** The following display appears:

```
Real Time Clock Utilities          Please wait....



        Real Time Clock Verification

(A)  Display Clock
(B)  Set Clock
(C)  Write non-volatile RAM of real time clock
(D)  Exit

Enter (1 char):
```

2. Type the desired character to verify the real time clock setting.

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Appendix C
Loopback Connectors

INTRODUCTION

This appendix shows the proper jumper connections for assembling the loopback connectors required to perform the parallel printer and communications (SIO and MDC) diagnostic tests described under "Field-Service Tests" in **Floppy-Based Diagnostics** - Chapter 4. The parallel printer loopback connector is a male DC-37P 37-pin connector (see Figure C-1) and the multidrop and SIO communications connector is a 9-pin female D-type (DE-9S) subminiature connector (see Figure C-2).

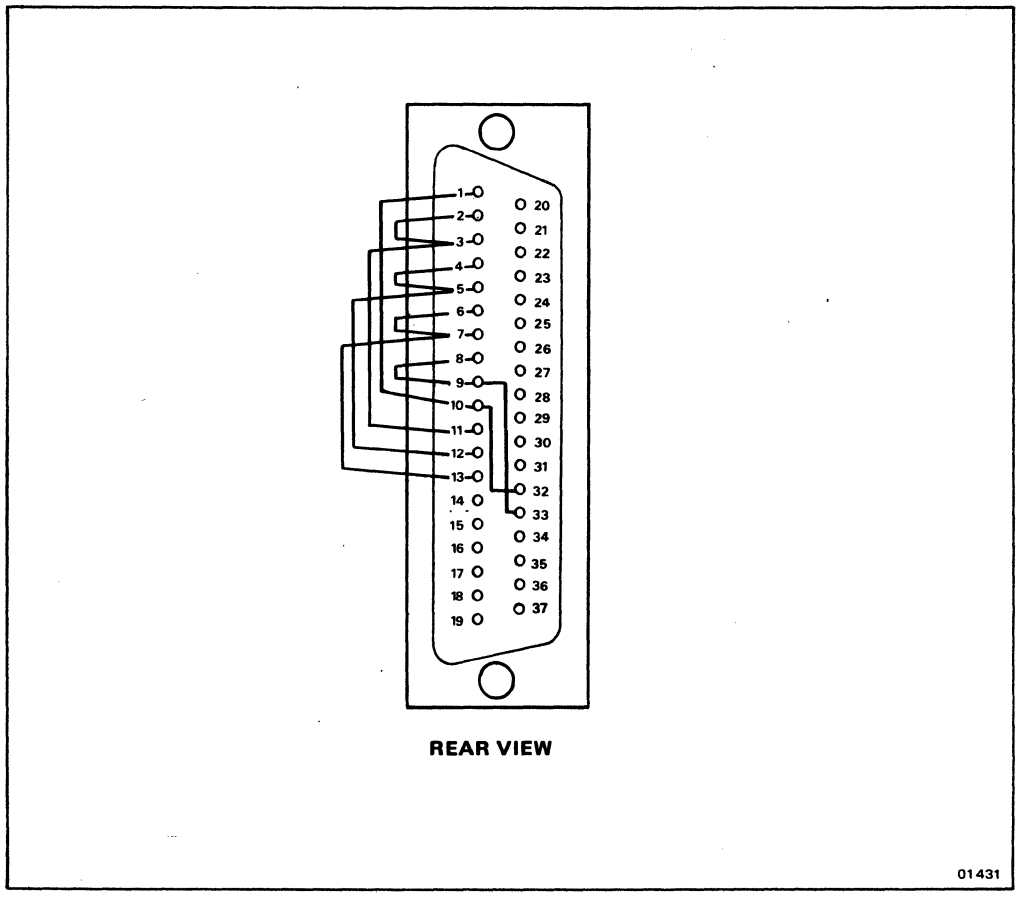

Figure C-1. Parallel Printer Port Loopback Connector

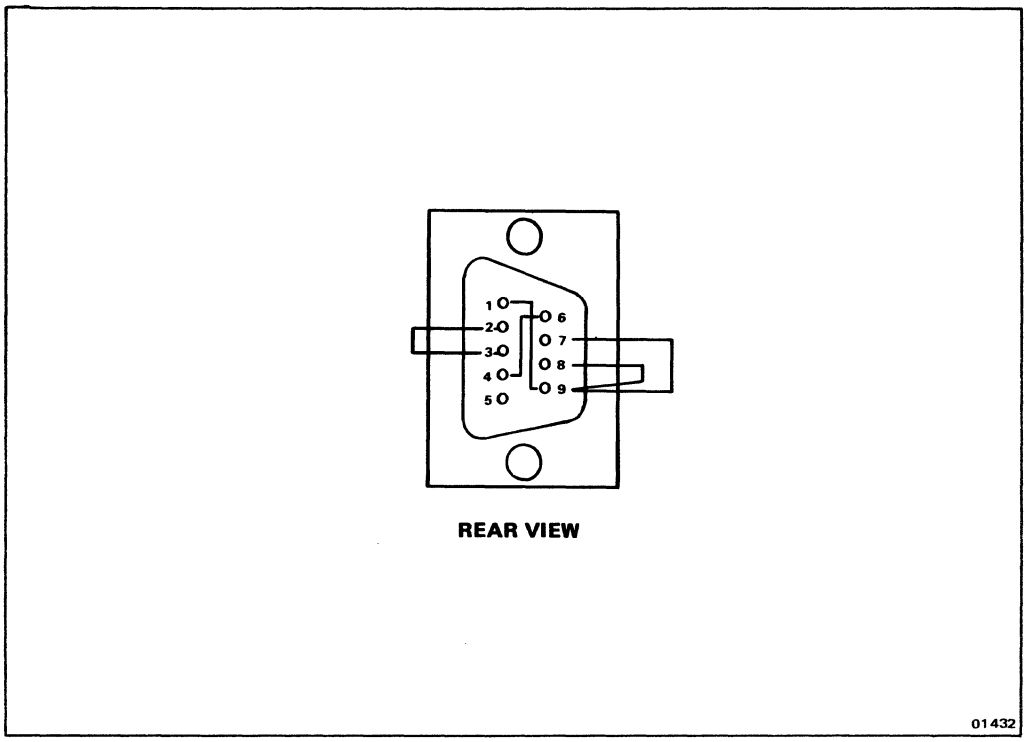

Figure C-2. Multidrop and/or SIO Communications Loopback Connector

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Appendix D
System Specifications

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INTRODUCTION

The electrical specifications listed in Table D-1 apply when the Altos 386 Series 2000 Computer System has been operating for at least 15 minutes at an ambient temperature between +40 and +95 degrees Fahrenheit (+5 and +35 degrees Celsius). The environmental and physical specifications are listed in Tables D-2 and D-3.

ELECTRICAL SPECIFICATIONS

Table D-1 lists the electrical specifications for the Series 2000 Computer System.

Table D-1. Electrical Specifications

Characteristic	Performance Requirement
Subsystem	
Central Processing Unit (CPU)	
Microprocessor	80386
Floating-Point Microprocessor	80387
Clock Frequency	
Internal	16 MHz
External	32 MHz
System Data Size	32 bits
System Address Size	26 bits
CPU Data Size	32 bits
CPU Address Size	32 bits
Data and Instruction Cache Data Block Size	32/64 bits
Data and Instruction Cache Memory Size	32K bytes
CPU to Memory Transfer Rate	14M bytes/second

Table D-1. Electrical Specifications (Cont.)

Characteristic	Performance Requirement
Subsystem (Cont.)	
System Memory	
Addressable Space	
Standard	4M or 8M bytes (256K x 1 bit dynamic RAM) per board
Optional	16M bytes, maximum
Transfer Word Length	Capable of 1, 2, 3, or 4 byte (32 bit) parallel transfers, and special 8 byte cache fill cycle
Access Time From:	
Memory Read Command	
Typical	220 nanoseconds
Maximum	550 nanoseconds (with refresh)
Memory Write Command	
Typical	60 nanoseconds
Maximum	360 nanoseconds (with refresh)
Cycle Time	
Memory Write Followed By Memory Read or Write	180 nanoseconds (Typically 281 nanoseconds)
Memory Read Followed By Memory Read or Write	Typically 400 nanoseconds
Multidrop Communications	
Microprocessor	80286
Clock Frequency	6 MHz
Total On-Board Ports	6
Multidrop	1
Async RS-232/WorkNet	1
Async/Sync RS-232	2
Async RS-232	2
RAM	512K bytes
Multidrop Protocol	
Access Protocol	CSMA (carrier sense, multiple access)/polled
Line Protocol	SDLC (synchronous data link control)

Table D-1. Electrical Specifications (Cont.)

Characteristic	Performance Requirement
Subsystem (Cont.)	
Multidrop Communications (Cont.)	
Data Transfer	
Maximum Rate/Distance	1M bit/second (DMA driven): 1500 feet per trunk segment. Extendable by repeaters to 4500 feet
Station Addresses	127 (XENIX limited, 254 available)
RS-422 Devices Per Trunk Segment	30 per 1500 foot trunk segment (90 maximum over full 4500 feet)
Maximum Logged-In Devices**	
Standard	32
Optional	64
SIO Communications	
Microprocessor	8086
Clock Frequency	8 MHz
Total I/O Ports	10
Configurable Synchronous Ports	2
Configurable Network Ports	1
RAM	
Standard	128K bytes
Optional	512K bytes
WorkNet Data Transfer	
Maximum Rate/Distance	750K bits/second: 2500 feet/trunk segment 1.4M bits/second: 1500 feet\trunk segment. Extendable to 4500 feet with 422 repeaters.

** Current XENIX operating system licensing limits.

Table D-1. Electrical Specifications (Cont.)

Characteristic	Performance Requirement
Subsystem (Cont.)	
File Processor/Controller	
Microprocessor	8086
Clock Frequency	8 MHz
Total External Ports	2
Parallel Printer Port	1
SCSI Port	1
Total Internal Ports	5
Tape	1
Floppy Disk	1
ESDI	3
Maximum Transfer Rates	
Tape	90K bytes/second
Floppy Disk	250K or 500K bits/second
Hard Disk (ESDI)	10M bits/second
SCSI	1.5M bytes/second
Printer	50K bytes/second

Table D-1. Electrical Specifications (Cont.)

Characteristic	Performance Requirement
Storage Devices	
(See **Storage Device Specifications** - Appendix E for additional drive specifications)	
Cartridge Tape Drive	
Number of Drives	1
Number of Tracks	9
Number of Channels	2
Capacity	60M bytes/cartridge
Backup Time	15 minutes (60M byte tape)
Media	1/4 inch Scotch DC-600A cartridge
Recording Mode	NRZI (nonreturn-to-zero invert)
Data Transfer Rate (Tape Speed)	90 inches/second
Format	QIC-24
Interface	QIC-36
Floppy Disk Drive	
Number of Drives	1 dual-speed, double-sided, double-density drive
Form Factor Size	5-1/4 inches
Formatted Size	
High Density	1.2M bytes
Low Density	720K bytes
Unformatted Size	
High Density	1.6M bytes
Low Density	1M byte
Data Transfer Rate	250K or 500K bits/second
Hard Disk Drives	
Number of Drives	1 to 3
Form Factor Size	5-1/4 inches

Table D-1. Electrical Specifications (Cont.)

Characteristic	Performance Requirement		
Storage Devices (Cont.)			
Hard Disk Drives (Cont.)			
ESDI			
Formatted Capacity			
80M Byte	73.0M bytes		
170M Byte	144M bytes		
Unformatted Capacity			
80M Byte	85.3M bytes		
170M Byte	170M bytes		
Interface	ESDI (enhanced small device interface)		
Data Transfer Rate	10M bits/second		
Average Seek Time (Includes Settling Time)			
80M Byte	28 milliseconds		
170M Byte	28 milliseconds		
Main Power Supply			
DC Output Voltages	+5	+12	-12
Accuracy	Adj.	±5%	±10%
Current (Continuous)			
Maximum	50 A	6 A	0.5 A
Minimum	5 A	0.1 A	0.05 A
Peak (300ms, Pulsed Load	N/A	6 A	N/A
Regulation (Line/ Load/Temp.)	±3%	±5%	±10%
Ripple/Noise (P-P)	50 mV	100 mV	150 mV
Overvoltage	Shutdown & cycle	Shutdown & cycle	N/A

Table D-1. Electrical Specifications (Cont.)

Characteristic	Performance Requirement
AC Power	
Line Voltage Range	
115 VAC (Nominal)	86-127 VAC
230 VAC (Nominal)	195-253 VAC
Line Frequency Range	47-63 Hz
Power Consumption	
Maximum	830 W
Continuous	550 W
Maximum BTU/Hour Output	2,833
Maximum Current (RMS)	6.4 A at 60 Hz, nominal 115 VAC line 3.6 A at 60 Hz, nominal 230 VAC line
Fuse Type	
115 VAC (Nominal)	10 A, normal-blowing type
230 VAC (Nominal)	5 A, normal-blowing type
Power Fail Status	Logic signal input from uninterruptable power source via UPS phone jack on rear panel. UPS monitor must be non-conducting when AC power is present and conducting when UPS is on
Voltage (Vce)	0.5 V maximum
Current (Ic)	1.6 mA DC

ENVIRONMENTAL SPECIFICATIONS

Table D-2 lists the environmental specifications for the Series 2000 Computer System.

Table D-2. Environmental Specifications

Characteristic	Performance Requirement
Temperature	
Operating	+40 to +95 degrees Fahrenheit (+5 to +35 degrees Celsius)
Storage	-4 to +140 degrees Fahrenheit (-20 to +60 degrees Celsius)
Gradient	Not to exceed 10 degrees Fahrenheit/hour (5 degrees Celsius/hour)
Maximum Wet Bulb	+78 degrees Fahrenheit (+26 degrees Celsius)
Relative Humidity	20 to 90% non-condensing

PHYSICAL SPECIFICATIONS

Table D-3 lists the physical specifications for the Series 2000 Computer System.

Table D-3. Physical Specifications

Characteristic	Description
Weight	
Computer	
Net	Approximately 68 to 86 lbs (31 to 38.5 kg)
Shipping	95 lbs (43 kg) maximum
TCU-8	
Net	Approximately 5 lbs (2.3 kg)
Shipping	8.5 lbs (3.9 kg) maximum
Dimensions	See Figure D-1

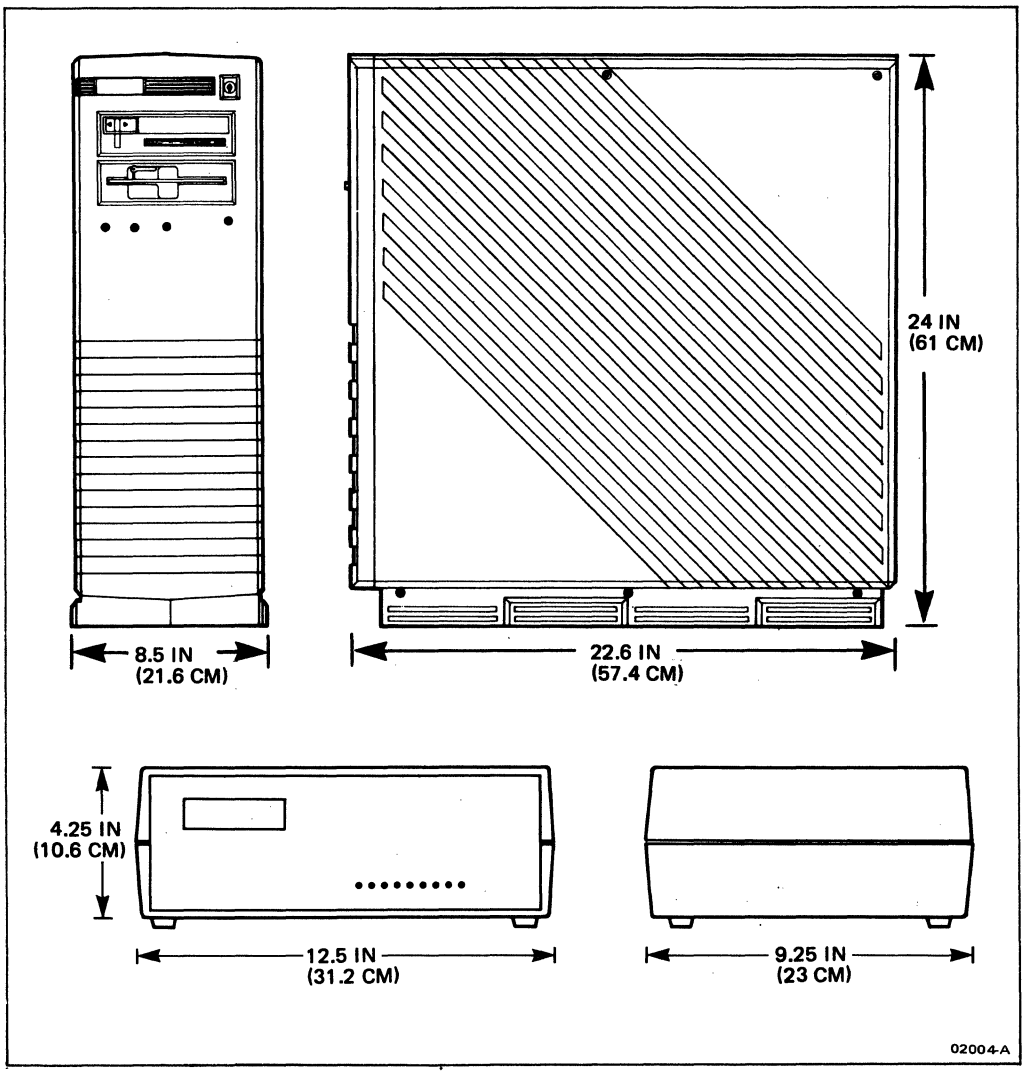

Figure D-1. Maximum Overall Dimensions

Appendix E
Storage Device Specifications

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INTRODUCTION

This appendix includes detailed specifications for the Altos 386 Series 2000 Computer System cartridge tape, floppy disk, and hard disk drives.

CAUTION

The drives specified in this appendix are those that have been tested and approved by Altos for use in this system. Altos is not responsible for the proper performance or subsequent service of any Series 2000 that does not have Altos-approved drives installed.

CARTRIDGE TAPE DRIVE

The cartridge tape drives installed in the Series 2000 are the Archive Scorpion or the WangTek Model 5000E. These drives use a 1/4 inch streaming cartridge tape packaged in a 5-1/4 inch footprint. The primary function of the cartridge tape drive is to provide backup for the hard disk drive.

The tape drive is connected to the controller board via a single 50-conductor ribbon cable to the backplane. The drive may be moved a maximum of 3 meters (9 feet 10 inches) away from the controller.

Electrical Specifications

The cartridge tape drive specifications listed in Table E-1 apply for both the Archive and WangTek drives.

Table E-1. Cartridge Tape Drive Specifications

Characteristic	Performance Requirement
Tracks	9
Channels*	2
Capacity (DC 600A)	60M bytes
Backup Time (DC 600A)	12 minutes
Recording Mode	NRZI (nonreturn-to-zero invert)
Recording Data Density	800000 bpi (bits per inch)
Encoding Method	4-to-5 RLL (run-length limited)
Flux Density	10,000 ftpi (flux transitions per inch)
Track Capacity DC 600A	6.6M bytes
Data Transfer Rate	90K bytes/seconds
Tape Speed	90 inches/second
Start/Stop Time	300 milliseconds

* Channels are defined as one write head gap followed by one read head gap.

As shown in Table E-1, when an industry-standard 1/4 inch magnetic tape cartridge is loaded into the tape drive 60M bytes of data can be stored or backed up in one 1/4 inch tape cartridge.

FLOPPY DISK DRIVE

The floppy disk drive installed in the Series 2000 is a Panasonic Model 475-2 or equivalent. The Panasonic drive is a half-height, 5-1/4 inch, double-sided drive that is selectable from low density to high density by a control signal from the interface.

Electrical Specifications

The specifications listed in Table E-2 apply to the Panasonic Model 475-2.

Table E-2. Floppy Disk Drive Specifications

Characteristic	Performance Requirement
Storage Capacity (Unformatted) Per Disk	
Low Density	1M byte
High Density	1.6M bytes
Storage Capacity (Unformatted) Per Track	
Low Density	6,250 bytes
High Density	10K bytes
Storage Capacity (Formatted) Per Disk	
Low Density	720K bytes
High Density	1.2M bytes
Heads	2
Tracks	80
Seek Settle Time	At least 18 milliseconds
Head Switching Time	At least 3.1 milliseconds
Write Gate Delay	0 millisecond after seek

ESDI HARD DISK DRIVES

The ESDI hard disk drives installed in the Series 2000 are the Hitachi Model DK 512-17 or the Micropolis Model 1355 or equivalent.

The operating system is programmed with drive informtion (number of heads, cylinders, etc.) when the drive is installed. This configuration stays with the system as long as the drive is not changed. Number of sectors per track and sector size is determined by the operating system.

Electrical Specifications

The ESDI hard disk drive specifications listed in Table E-3 apply for the Micropolis Model 1353, Hitachi Model DK 512-17, and the Micropolis Model 1355.

Table E-3. ESDI Hard Disk Drive Specifications

Characteristic	Performance Requirement
Micropolis Model 1355	
Storage Capacity	
Unformatted	170.6M bytes (170M bytes)
Formatted	146.0M bytes
Sectors/Track	35
Cylinders	1024
Tracks	8,192
Heads	8
Track Skew	4
Sector Interleave	0
Bytes/Sector	512
Precomp Track	None
Data Transfer Rate	1.25M bytes/second
Recording Density	Not applicable
Recording Method	RLL (2-7)
Transfer Method	NRZ (non-return to zero)
Seek Time (Includes Settling Time)	
Single Track	6 milliseconds, maximum
Average	28 milliseconds, maximum
Full Stroke	62 milliseconds, maximum
Interface	ESDI (enhanced small device interface)
Technology	Winchester

Table E-3. ESDI Hard Disk Drive Specifications (Cont.)

Characteristic	Performance Requirement
Hitachi Model DK 512-17	
Storage Capacity	
Unformatted	172.3M bytes (170M bytes)
Formatted	144M bytes
Sectors/Track	35
Cylinders	823
Tracks	8,230
Heads	10
Track Skew	4
Sector Interleave	0
Bytes/Sector	512
Precomp Track	None
Data Transfer Rate	1.215M bytes/second
Recording Density	18,500 bpi/925 tpi
Recording Method	RLL (2-7)
Transfer Method	NRZ (non-return to zero)
Seek Time (Includes Settling Time)	
Single Track	6 milliseconds, maximum
Average	23 milliseconds, maximum
Full Stroke	45 milliseconds, maximum
Interface	ESDI (enhanced small device interface)
Technology	Winchester

Table E-3. ESDI Hard Disk Drive Specifications (Cont.)

Characteristic	Performance Requirement
Micropolis Model 1353	
Storage Capacity	
Unformatted	85.3M bytes (80M bytes)
Formatted	73.0M bytes
Sectors/Track	35
Cylinders	1024
Tracks	4,096
Heads	4
Track Skew	4
Sector Interleave	0
Bytes/Sector	512
Precomp Track	None
Data Transfer Rate	1.0M bytes/second
Recording Density	Not applicable
Recording Method	RLL (2-7)
Transfer Method	NRZ (non-return to zero)
Seek Time (Includes Settling Time)	
Single Track	6 milliseconds, maximum
Average	28 milliseconds, maximum
Full Stroke	62 milliseconds, maximum
Interface	ESDI (enhanced small device interface)
Technology	Winchester

Appendix F
115/230 VAC Conversion

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INTRODUCTION

This appendix provides the procedure for converting the Altos 386 Series 2000 to 115 or 230 VAC nominal line voltage operation.

NOTE

Altos recommends that the procedures in this chapter be performed by qualified service personnel.

SELECTING 115/230 VAC OPERATION

Perform the following procedure to select 115 or 230 VAC operation for the Series 2000. Converting to 115 or 230 VAC nominal operation requires a jumper change to the main power supply.

1. Turn off the Series 2000 power and unplug the AC power cord. (See "Controls, Connectors, and Indicators" in **System Description** - Chapter 1 for the locations of the power switch and power cord connectors.)

2. Remove the front panel as described in **Removal/Replacement** - Chapter 6.

3. Remove the right-hand side panel as described in **Removal/ Replacement** - Chapter 6.

4. Connect the main power supply line-voltage jumper to select 115 or 230 VAC nominal operation as shown in Figure F-1.

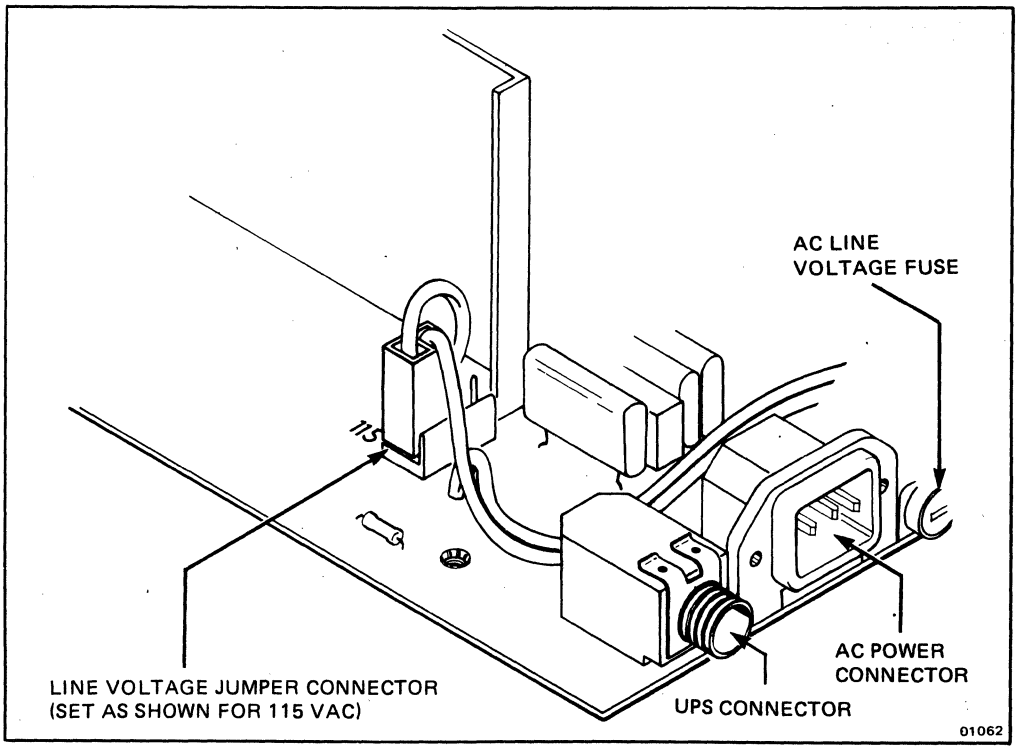

Figure F-1. 115/230 VAC Selection (Main Power Supply)

5. Replace the AC line voltage fuse with the proper fuse for 115 or 230 VAC operation. Refer to **System Specifications** - Appendix D for the proper fuse rating.

Appendix G
Multidrop Cables and Terminators

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INTRODUCTION

This appendix contains instructions and wiring diagrams for making your own multidrop interconnect cables, drop cables, and terminators. Also included is information on how to order cables from a cable vendor. Before ordering cables or connectors, check the appropriate back panel connector on your system to make sure the number of pins on the Altos side matches the diagram you are using.

NOTE

To maintain the FCC Class A rating of your system, make sure all interface cables have a grounded shield. Connect cables securely to the system unit and the peripheral device both electrically and mechanically.

SELECTING THE RS-232 CABLE LENGTHS

The maximum recommended length of cable depends on the baud rate set for the terminal or printer as shown in Table G-1.

Table G-1. Maximum Recommended Cable Lengths

Maximum Recommended Distance	Baud Rate
60 feet	19200
125 feet	9600
250 feet	4800

Notice that the longer the cable, the lower the baud rate. For example, if you set a terminal at 9600 baud, the maximum cable length is 125 feet. If you exceed these guidelines, you may lose data.

Table G-2. Cable Manufacturer's Part Numbers

Description	Generic	Cinch	AMP P/N
15-pin female connector	DA-15S	DA-15S	205205-2 (shell) 66505-4 (crimp pin) 66569-3 (solder pin)
15-pin male connector	DA-15P	DA-15P	205206-3 (shell) 66507-4 (crimp pin) 66570-3 (solder pin)
15-pin hood		745172-1	

MAKING MULTIDROP CABLES

The following cable diagrams will help you construct multidrop cables. For best results, use lowcapacitance cable (8.8 pF/ft, such as Belden 9184) for all interconnect cables.

The cabling scheme uses a dual-twisted pair interconnect. One pair carries the clock; the other carries the data. A third conductor provides the signal ground which the line drivers and receivers use as a common reference.

A minimal interconnect cable consists of 2-twisted pairs and a shield connected to signal ground. However, a better approach is to use 2-twisted pairs, a signal ground wire, and an overall shield connected to chassis ground. The second method provides better external noise immunity, and radiates less noise.

The signal lines (both clock and data) must be terminated with 150 ohm resistors at each end of the interconnect line.

In most installations, the recommended cable types are Belden type 9184 (2-pair and shield) or Belden type 8133 (3-pair and shield). For the interconnect backbone cable, it is more desirable to use Belden 9184 due to its superior line characteristics. Belden 8133 is more desirable for drop cables because of its superior shielding, electro-static discharge (E.S.D.) protection, and smaller diameter which makes routing easier.

If local fire codes require using teflon coated cabling, use Belden 89729 for both drop and interconnect cabling. Belden 89729 is approved by the National Electrical Code for plenum use. Use of teflon cables **reduces** the maximum allowable distance for multidrop interconnect segments to 1000 feet instead of 1500 feet (a "segment" is the maximum trunk length without repeaters, or the distance between two repeaters). This restriction is due to the increased capacitance of the teflon cabling.

IMPORTANT! To reduce problems due to line reflections, use the following ratios when planning cable lengths.

- the **minimum** ratio between the drop cable length and interconnect cable length to the next drop should be 1-to-3. (For example: a 20-foot drop cable requires at least a 60-foot interconnect cable to the next 20-foot drop. If you have many multidrop terminals, or networked systems in a close area, use 1-foot drop cables.)

- the **optimum** ratio between length of drop cable and length of interconnect cable to next drop should be 1-to-5.

Table G-3. Cable Specifications

Cable Type	Belden 9184	Belden 8133	Belden 89729
Conductors	2 pair + shield	3 pair + shield	2 pair + shield
Type of Shield	Foil	Foil + braid	Foil
Gauge	22 a.w.g.,solid	28 a.w.g.,stranded	24 a.w.g.,stranded
Impedance	150 ohms	120 ohms	100 ohms
DC Resistance	16 ohms/1000 ft	65 ohms/1000 ft	24 ohms/1000 ft.
Capacitance	8.8 pF/ft	11.0 pF/ft	12.5 pF/ft
Cable Diamater	.385 inch	.270 inch	.284 inch
Jacket Color	Black	Gray	Red Teflon
Max. Length/Line	1500 ft	1000 ft	1000 ft

Table G-4 lists the 15-pin connector pinouts. Multidrop stations have a type DA-15S female 15-pin connector. The multidrop mating cable has a male DA-15P type plug.

Table G-4. 15-Pin Cable Pin Assignments

Pin No.	Signal Name	Function
1	CG	Chassis (protective) ground
2	DAT+	Data + Bidirectional serial data
4	CLK+	Clock + Timing for serial data
10	DAT-	Data - Complement of DAT+
12	CLK-	Clock - Complement of CLK+
15	SG	Signal ground, signal common

Making a 15-to-15 Pin Drop Cable

The cable wiring diagram shown in Figure G-1 allows you to connect a 15-pin device to the multidrop interconnect line. A 20-foot drop cable and a 1-foot drop cable are available through your Altos dealer or distributor.

One end of this cable has a male 15-pin connector. The other end has a female 15-pin connector. **Do not allow the signal ground wire to come into contact with the connector shell.** Wire colors are shown for both Belden 9184 and Belden 8133 cabling.

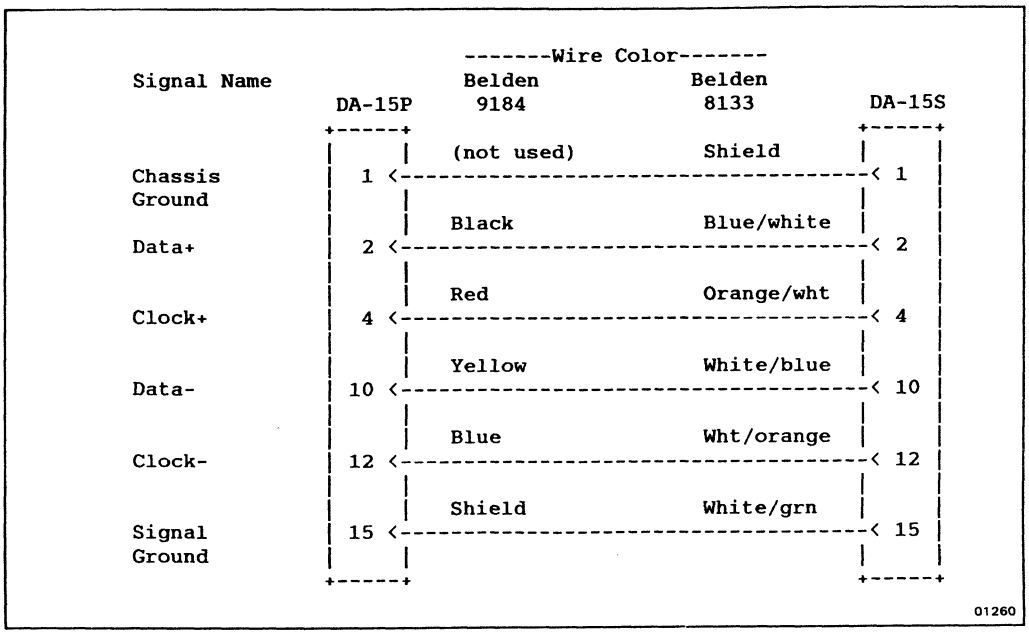

Figure G-1. Wiring Diagram For a 15-to-15 Pin Drop Cable

Making an Interconnect Cable

The cabling wiring diagram in Figure G-2 shows you how to construct an interconnect cable. Each end of this cable has a male 15-pin connector.

It is best to use low-capacitance cable (8.8 pF/ft, such as Belden 9184) for all interconnect cabling. **Do not allow the signal ground wire to come into contact with the connector shell.** Wire colors are shown for both Belden 9184 and Belden 8133 cable.

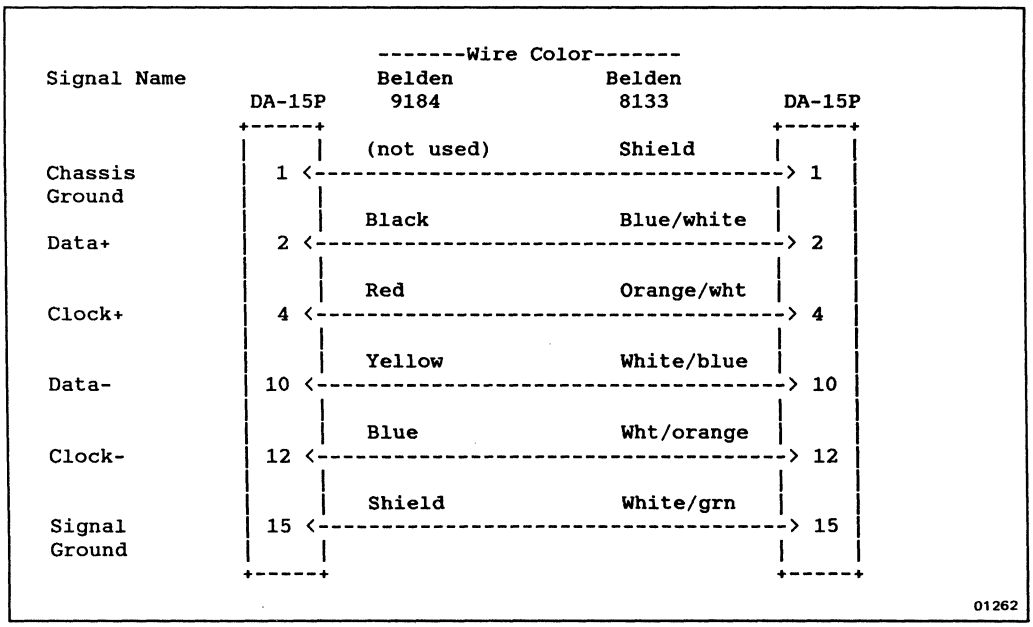

Figure G-2. Wiring Diagram For an Interconnect Cable

Making a Terminator

The wiring diagram in Figure G-3 shows you how to construct a terminator for the interconnect line. Only two terminators are required per installation, no matter how many interconnect segments or repeaters are used (the repeater device has internal line terminators.)

The terminator consists of a male 15-pin plug which contains two 150-ohm, 1/4-watt carbon resistors.

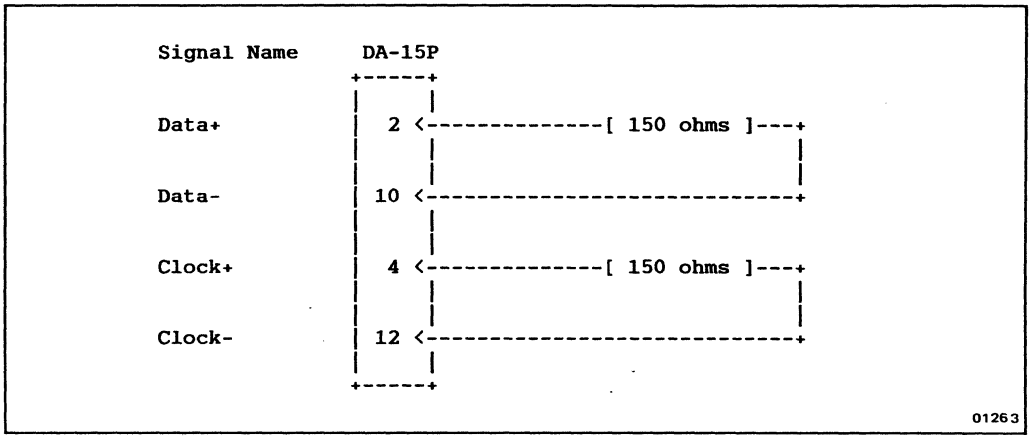

Figure G-3. Wiring Diagram For a Terminator

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Appendix H
Power Consumption Chart

INTRODUCTION

Table H-1 lists the power consumption for each of the available Series 2000 configurations. The main power supply currently installed in the system is a 340 watt switching type.

Table H-1. Power Consumption Chart (340 Watt Power Supply)

	DC Power Consumption						
	+5 Volts*		+12 Volts**		-12 Volts		
Standard Boards	Amps Avail.	Amps Used	Amps Avail.	Amps Used	Amps Avail.	Amps Used	Board Slot Location
16 MHz 80386 CPU	37.0	5.5	5.9	0.1	1.4	0.1	A
2 MB Memory II	33.0	4.0	5.9	N/A	1.4	N/A	B-E
4 MB Memory II	***	5.2	****	N/A	****	N/A	B-E
8 MB Memory II	***	5.6	****	N/A	****	N/A	B-E
SIO (32/128 KB)	***	3.7	****	0.2	****	0.2	
MDC	28.0	5.0	5.3	0.6	1.2	0.2	F
File Processor (128 KB)	22.0	6.0	5.3	N/A	1.2	N/A	G
Controller (ESDI)	18.5	4.0	4.9	0.4	1.2	N/A	H
Tape Drive	17.9	0.6	2.9	2.0	1.2	N/A	
Floppy Drive	17.4	0.5	1.9	1.0	1.2	N/A	
Hard Disk Drive(s)	Drive modules are hard-wired to AC line source and do not load main power supply.						

* The 42.5 amps in the +5 VDC supply is 15% less than the rated 50 amps as specified for the 340 watt power supply in order to provide a safe margin.

** The +12 VDC is rated at 6 amps continuous and 7 amps for 300 ms, pulse load.

*** Depends on configuration.

**** No added load.

Glossary

A

Accessing The act of entering data into or retrieving data from a memory device.

Application Program
A program written to perform a specific user task as opposed to development or utility programs.

Architecture
A design or orderly arrangement.

ASCII American Standard Code for Information Exchange. A standard 7-bit digital code (8 bits including parity check) for each of 96 graphic characters and 32 control characters.

Associating Cache
A type of memory in which data is retrieved by comparing a key against the contents of each location rather than first accessing the address of each location. The key is a copy of all or part of the data being retrieved. This type of search is faster over limited amounts of data.

Asynchronous
A nonclocked method for data transmission where the interval between the data is variable. For RS-232, the transmitted characters are preceded by a start bit and followed by a stop bit which permits a variable interval between characters.

B

Backplane A printed circuit board that contains the system bus and provides the interconnections between the PCBs, main power supply, and drives. The PCBs and drives plug into the backplane.

Bandwidth Relates to the speed of transmission through a channel; the greater the bandwidth, the higher the transmission speed (usually measured as the baud rate).

Baud The number of signal events per second. One baud equals one bit per second in a train of binary signals.

Bit-Serial Format
A method of sequentially transferring a contiguous set of bits, one at a time, over a single line.

Block-Transfer Mode
A mode where the I/O processor moves a block program.

Boot Prepare the computer for use by loading the operating system into memory from either a floppy disk or a hard disk.

Breakpoint
A specific stopping point in a program (usually indicated by a breakpoint flag) that interrupts the program to permit checking, correcting, or modifying the program before continuing execution.

Buffer A device inserted between two other devices or program elements for the purpose of matching the electrical interfaces. Buffers are also used for matching two different data rates by providing intermediate storage.

Burst Mode
A file processor mode that causes data transfer in short bursts followed by periods of inactivity. This mode prevents the file processor from locking the system bus for excessive periods of time.

Bus Master
The device controlling the current system bus transactions.

Byte-Select Field
Refers to the particular byte or bytes within a block of memory which is to be read/written to the cache memory.

Byte-Swap Logic
A logic concept where the two bytes in a 16-bit word are interchanged (swapped).

C

Cache Memory
A high-speed low-capacity memory used as a buffer between the CPU and system memory to allow faster access for instructions and data.

Call Refers to the process of bringing a program, routine, or subroutine into effect by specifying the entry conditions and jumping to an entry point.

Cascade Refers to two or more similar devices arranged in tandem; the output of one connected to the input of the other.

CIO Counter/Input/Output. A device that acts as a general-purpose counter/timer to provide bit set/test functions and acts as an interrupt controller for miscellaneous inputs.

Code A system of characters and rules for representing information.

Coercivity
A measure of how tightly two adjacent bits can be recorded on magnetic media and still be read; the higher the coercivity, the better the quality.

Coherency On the CPU PCB, the cache memory is considered coherent when the data in the cache is in agreement with the data in system memory. Thus, the cache can be trusted by the CPU.

Complement
The opposite of a given quantity.

Concatenate
To join two or more character strings or bits end-to-end to orm a larger word or string.

Concurrent
Refers to the handling of multiple instructions or the operations of different instructions simultaneously.

Context Switching
Refers to switching from one process to another. Context switching is per formed by the operating system.

Contiguous
Sharing a common boundary or edge.

CPU Central Processing Unit. The primary functioning device of the computer that synchronizes the operation of the computer system. It fetches control instructions stored in memory and then decodes, interprets, and performs the programmed instructions. The term CPU is used to describe a single integrated circuit (microprocessor) and also the expanded CPU subsystem (PCB) that contains memory, timing, control logic, and communications interface to other subsystems.

CRC Cyclic Redundancy Check. A method for detecting transmission errors in serial data streams. A check bit is appended to the data stream and then the resulting bit stream is divided by a selected poly nomial. If there are no errors, the remainder should be zero.

Cued Refers to waiting for service based on the order of arrival.

D

Daisy Chain
Refers to an interconnect method where several devices share the same signal path. The daisy chain method reduces the cost of interconnection and requires that the devices timeshare the signal path.

Data Block
A contiguous group of data bytes.

Data Pattern
A sequence of characters that are repeated throughout a memory area.

Debugger A software program that performs tests of computer routines for locating software errors and correcting them.

Decode To disassemble or translate a code into its meaning. For example, a decoder assigns a one bit meaning to each of the eight possible threebit codes.

Decrement To decrease the value of a number.

Delimiter A character that limits a string of characters or separates and organizes items of data.

Development System
A computer system especially designed for developing firmware and software.

Diagnostics
Refers to a user-inserted test program for isolating hardware malfunctions to a subsystem or major circuit.

Direct Map
Refers to a type of storage medium that provides dynamic allocation of memory.

DMA Direct Memory Access. A method to gain direct access to system memory without involving the CPU.

Download The process of moving a program from the primary to the secondary controlling device, which results in the secondary device becoming activated.

E

Execute The process of interpreting an instruction and performing the indicated operation(s).

F

False Refers to the zero (0) or low state in Boolean algebra.

Fileserver
A device that manages controllers which, in turn, create, delete, or retrieve data files from storage devices, such as disks or tapes.

Firmware Refers to software programs or instructions that have been permanently stored in a ROM control block.

Flag An indicator, usually a single binary bit, used to inform a later section of a program that a condition had occurred.

Footprint Refers to the physical space provided in the chassis to accommodate a subassembly (module).

Formatted Disks are considered formatted after a pattern has been written on the disk that divides the disk storage area into addressable sectors.

Fragmentation
A condition resulting from some dynamic storage-allocation algorithms, in which unallocated storage is dispersed in many small areas.

Full-Duplex
Refers to an operation that allows simultaneous communication in both directions between two points.

H

Half-Duplex
Refers to an operation that allows communication in either direction, but not simultaneously, between two points.

Handshake
Exchange of predetermined signals between a transmitting and receiving device to establish synchronization.

Hit Refers to a cache search operation. When an address in the tag memory matches a read address from the CPU, a cache hit occurs which indicates that the data wanted by the CPU is stored in the cache memory. See Miss.

Host Refers to the primary or controlling device.

I

Increment To increase in quantity or value.

Initialize To set a program, system, or device to an original state.

Interactive Diagnostics
Refers to diagnostics procedures where the user can communicate directly with the operating program.

IOP Input/Output Processor. Refers to a device that is capable of moving data between main memory and peripheral devices while the CPU is performing other tasks.

IPL Initial Program Load. Refers to the program stored in the PROM that performs local power-up and initialization of the file processor and communications PCBs during the boot process.

L

LAN Local Area Network. A system for interconnecting computers within a limited area using data-link control to establish paths, manage message transactions, and free lines for other users. WorKnet is an LAN system.

Latency The time required by the computer to deliver information from memory. In a disk drive, the average time required for a sector to come under the read/write head once the heads are on track (for a 3600 rpm disk, latency is 8.33 milliseconds).

Long Word A 32-bit unit of information.

Loop A self-contained series of instructions in which the last instruction can modify and repeat itself until a terminal condition is reached.

Loopback Mode
A mode of operation where transmitted data is returned to the sending end for comparison with the original data.

M

Macro A form of instruction used to generate a debugging program testing capability that is completely under the user's control.

Main CPU The central processing unit on the CPU PCB.

Main Console
The console connected to serial communications port 0 from which diagnostic testing is performed. Also called master or system console.

Map A listing of the variable names, array names, and constants used by the program, with their relative address assignments.

Maskable Interrupt
A single interrupt request input that can be masked by software with the resetting of the interrupt-enable status (flag) bit.

Mass Storage Device
Refers to a peripheral storage device with a large storage capacity (magnetic disk and tape).

Master Refers to a controlling device (console, CPU, etc.).

Minicomputer
Refers to the classification of computers with higher performance than microcomputers. Generally these computers are characterized by a proliferation of high-level languages, operating systems, and networking methodologies.

Miss Refers to a cache search operation. When an address stored in the tag memory does not match the read address from the CPU, a cache miss occurs which indicates that the data wanted by the CPU is stored in system memory and not in the cache memory. See Hit.

Model C Compiler
A high level programming language designed to optimize run time, size, and efficiency. C compiler supports the basic data types, such as bytes, long and short integers, floating-point numbers, and pointers to all data types.

Modem Refers to a MODulation/DEModulation device that modulates digital signals to enable the computer to communicate over telephone circuits.

MULTIBUS Refers to a type of intel bus similar to the 32-bit bus used by the Altos 1086/2086.

Multisector Transfer
A transfer of more than one sector at a time.

N

Networking
Refers to the interconnecting of computers through network communications channels.

NMI Nonmaskable Interrupt. An external interrupt that cannot be ignored by the microprocessor.

Nonmaskable Interrupt See NMI.

O

Offset Field
Refers to the cache memory address of the block location within a page of memory.

Operating System
A basic group of programs that perform computer debugging, input/output, accounting, compilation, and storage assignment tasks.

Out-Of-Bounds Error
A logical address, for which no matching physical address is found, generates an out-of-bounds error.

Overlapped Seeks
A hard disk controller with this capability can initiate a seek on a second (or third) drive before the first drive has completed a seek operation.

P

PAL Programmable Array Logic. An array of logic circuits that are custom programmed by the factory to process input signals.

Packet Refers to a group of bits, including data and control elements, that are transmitted as a whole.

Page A subdivision of physical memory into equal sized blocks called frames. The logical address space of a task is divided into pages. The operating system controls the allocation of pages into page frames. Paging is used in virtual memory systems.

PCB Printed Circuit Board. Sometimes called etched circuit board or printed circuit assembly (PCA).

Peripheral
Refers to an external device that enables the computer to communicate with the outside world, but is not part of the basic computer unit (storage devices, modems, terminals, etc.).

Phase-Locked Loop
A circuit that is synchronized in phase and frequency with a recieved signal.

Physical Address Space
Refers to the addressable storage sites or locations available in a memory device.

Pointer A word that gives the address location of another memory location.

Port A collection of individual I/O lines. Device terminals that provide electrical access to a system or circuit.

Power-Up Refers to the orderly initialization of the CPU at power-on time so that the proper sequence of events can occur.

Protocol A set of conventions, or rules, between communicating processes relating to the format and content of messages to be exchanged.

R

Real Time Refers to a task that must be started and completed within a certain time limit or the task will fail.

Refresh A process of constantly reactivating or restoring information that decays or fades when idle. Pertains to dynamic memory devices.

Register A memory device capable of containing one or more computer bits or words. A register has zero-memory latency time and negligible memory access time.

Remote Diagnostics
Refers to a method for diagnostic testing the computer system via a communications modem through a main or master console located some distance away.

Reset To restore a storage device to a prescribed state.

Resident Program
Refers to a program that is permanently located in memory.

Ripple Slang for shifting data patterns (used by diagnostics).

RS-232 The Electronic Industries Association (EIA) interface standard for transmitting asynchronous binary serial data between the computer and data terminal equipment (printers, terminals, modems, etc.).

RS-422 The Electronic Industries Association (EIA) interface standard for transmitting high-speed digital data between the computer and data terminal equipment (printers, terminals, modems, etc.).

S

Scatter Loading
A process for loading a program into system memory in such a way that each section or segment of the program occupies a single connected memory area (page), but the several sections of the program need not be adjacent to each other.

SCC Serial Communications Controller. A dual-channel multifunction peripheral component designed to satisfy a wide variety of serial data communications requirements. The SCC is capable of handling synchronous or asynchronous protocols.

SCSI Small Computer System Interface. Generally used for connecting additional peripheral devices to a computer.

Scroll Refers to the method of viewing extra lines or pages of non-displayed data on a terminal by pressing the appropriate keys.

SDLC Synchronous Data Link Control. A protocol for the management of data transfer via a data communications link.

SDX Service Diagnostics. Refers to a field service diagnostics program contained on a floppy disk included with the 1086/2086.

Sector Refers to the short segments (cones) in which tracks of data are stored on a floppy disk.

Segmented
Refers to a program that is divided into an integral number of parts, each of which performs a part of the total program and is short enough to be completely stored in memory.

Semaphores
Conditional input/output used to synchronize the data transfer between the computer and a peripheral device.

Serial Port
Refers to an I/O port through which data is transmitted and recieved in a digit-by-digit time sequence.

Single-Address Mode
A method of transferring data, used by the Hitachi HD68450, in which data is transferred around the DMA integrated circuit rather than through it. In contrast, dualaddress mode first transfers data into the DMA integrated circuit and then to the destination (sometimes called fetch deposit cycle).

Software
Refers to the programs or routines, usually supplied on a disk or in software documents, that are prepared to simplify programming and computer operations (operating systems, assemblers, compilers, utility, and application programs).

Source Code
Refers to the high level code in which the software is written. Source code is generally considered proprietary.

Stack A reserved area of memory where the CPU auto matically saves the program counter and the contents of working registers when a program interrupt occurs.

Standalone
Refers to an independent system that does not depend on another system for its operation.

Strobe A pulse used for loading registers or flipflops.

Subassembly
Refers to a subordinate assembly that comprises a part of the computer system. Subassemblies include mass storage devices, power supplies, backplane, and plug-in PCBs.

Subsystem
Refers to the portion of a subassembly that performs one of the major system functions. Subsystems include the major circuits contained on the plug-in PCBs.

Synchronous
Refers to an operation that occurs at regularly timed intervals, usually synchronized by a clock.

Syntax Refers to a the structure or arrangement of characters, such as spaces and commas, that gives a language control information.

System Console
Also called the master or main console. Refers to the controlling terminal or console for performing diagnostic tests or programming operations.

System Memory
Refers to the internal main memory contained on the memory PCB.

T

Tag Field
A portion of a data or address word that contains the key to the word. The key is used to locate the word during a cache search operation. Sometimes called key field.

Tag Memory (RAM)
A random access memory which contains the necessary address information for determining the presence of data in the CPU cache memory.

Throughput
Refers to the speed with which problems, programs, or segments are performed by the system.

Timeout Refers to the time interval allotted for certain operations to occur before the system is interrupted and must be started again.

Time Slice
Refers to a portion of the total available time allocated to a particular task to allow other tasks to be performed.

Toggle Refers to a change of states.

Transceivers
A device that can both transmit and recieve signals.

Translation Memory
Also called translation table memory. Refers to the memory device that correlates relocated addresses with real addresses.

Transparent
Refers to the moving of information through a device in such a way that the content of the data does not affect the processing operation.

True Refers to the one (1) or high state in Boolean algebra.

U

UPS Uninterruptable Power Source. Refers to a device that automatically switches to utility power when the AC line power is interrupted without disturbing computer operation.

Unformatted
Refers to magnetic media (tapes or disks) that have no data and no track or sector format information stored on them.

Universal Parameter Block
A temporary storage area in system memory used for passing instructions and status between the CPU and its slave microprocessors.

V

Vector Interrupt
A type of interrupt that uses a vector (pointer) which points to the starting address of a specific interrupt service routine.

Virtual Address Space
The total memory space allocated on peripheral storage devices that maps directly into system memory.

Virtual Memory
Refers to a technique which allows the programmer to use a larger address space than is available in system memory. The operating system automatically uses secondary memory (usually a disk) to store and retrieve parts of the currently executing program when the address space in system memory is exceeded.

W

Wait State
Refers to the insertion of a state while waiting for an event to occur.

Window A rectangular portion of memory which acts as a logical subterminal.

Word A 16-bit unit of information usually occupying one storage location in memory.

Write-Through
Refers to a write operation whereby the CPU writes to system memory and to cache memory in the same operation. Thus, it appears that the CPU is writing through the cache memory. Write-through is one of the methods required to assure that the cache memory matches the system memory.

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NOTE

The local I/O space is not fully decoded. Accessing I/O addresses other than those described in Table 3-20 is not recommended.

Multi-Drop

Table 3-20. I/O Port Assignments

Port	R/W	Function
0000h-7FFFh	R/W	System I/O ports
		SCC0
8000h	R/W	Channel B control registers
8002h	R/W	Channel B data register (port 0 - console)
8004h	R/W	Channel A control registers
8006h	R/W	Channel A data register (port 1)
		SCC1
8100h	R/W	Channel B control registers
8102h	R/W	Channel B data register (port 2)
8104h	R/W	Channel A control registers
8106h	R/W	Channel A data register (port 3)
		SCC2
8200h	R/W	Channel B control registers
8202h	R/W	Channel B data register (port 4 - WorkNet)
8204h	R/W	Channel A control registers
8304h	R/W	Channel A control

Multi-Drop

Table 3-20. I/O Port Assignments (Cont.)

Port	R/W	Function
		SCC3
8300h	R/W	Channel B control registers
8302h	R/W	Channel B data register (port 5 - multidrop) registers
		CIO (Miscellaneous I/O Control Bits and Counters/Timers)
8400h	R/W	Port C data register (status bit inputs)
8402h	R/W	Port B data register (output flags)
8404h	R/W	Port A data register (misc. input bits)
8406h	R/W	Control registers for CIO
		8259 PIC (Prioritization for ADMA Multiplexer Channel)
8500h	R/W	Command register(s)
8502h	R/W	Status register(s) and interrupt mask register
		DMA Controller
8600h-86FEh	R/W	DMA controller - ADMA registers (See **82258 data sheet** for details)
8700h	R	Null device for ADMA
8700h	W	System memory page register (provides memory address bits A18-A25 during accesses to system memory)

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